

Project code : 91.4F501.001
PCB P/N : 05232
Revision : SD

CLK GEN
ICS954305
3

Intel CPU
Yonah/Merom
4,5

DDRII 533/667 Slot 0
11

DDRII 533/667 Slot 1
11

Calistoga
GM
6,7,8,9,10

RGB CRT
13

LVDS
14

SVIDEO
13

PCIE x 16

1394
23

1394
23

SD/SDIO/MMC
MS/MS Pro/xD₃

Ricoh
R5C832
CardReader
22,23

RJ45
CONN
25

10/100 NIC
Intel 82562ET

ICH7-M
15,16,17,18

USB 2.0

SATA

PATA

LPC Bus

CAMERA
30

BLUE
TOOTH
30

USB x 3
21

HDD
20

ODD
20

RJ11
CONN
25

MODEM
AMOM
WAKIKI
AUDIO CODEC

INTERNAL
ARRAY MIC

MIC IN

LINE OUT

SPDIF

OP AMP
APA2031
28

2CH
SPEAKER

Ricoh
R5538
26

New Card
26

Mini-Card
802.11a/b/g
24

Mini-Card
24

KBC
ENE KB3910SF
29

Capacity
Button

Touch
Pad
30

Int.
KB
30

CIR
30

Thermal
& Fan
G792
19

Flash ROM
1MB
31

DOCK

CRT MIC IN LINE OUT SPDIF TVOUT 10/100 Ethernet CIR

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

Calistoga Strapping Signals and 125V Spread Spectrum Select Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6		0=Moby Dick 1=Calistoga
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	Reserved	
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

History
11.18.2004: mini card not ready

125V Spread Spectrum Select

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+-0.3
1	0	0	1	+-0.4
1	0	1	0	+-0.5
1	0	1	1	+-0.6
1	1	0	0	+-0.8
1	1	0	1	+-1.0
1	1	1	0	+-1.25
1	1	1	1	+-1.5

PCI Routing

	IDSEL	IRQ	REQ/GNT
R5C832	25		0

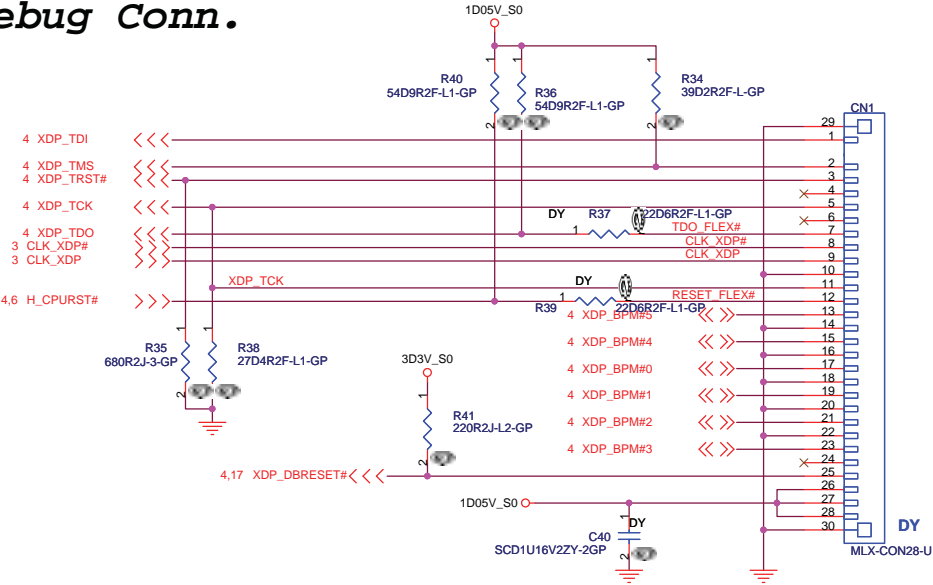
ICH6M Integrated Pull-up and Pull-down Resistors

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT,ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ITP Debug Conn.

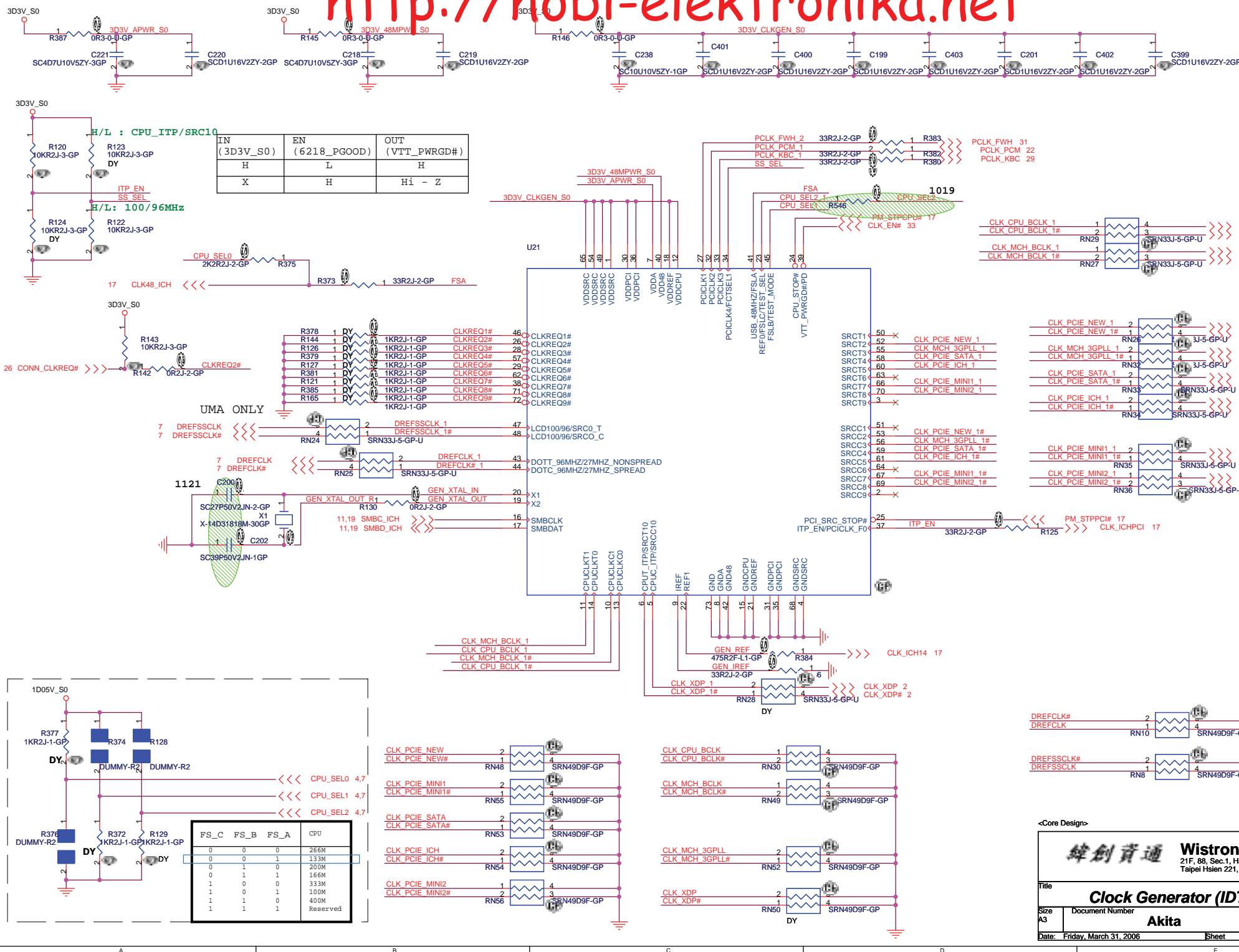


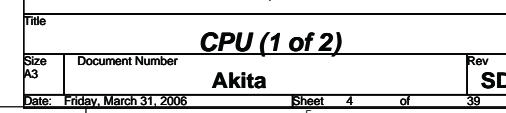
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

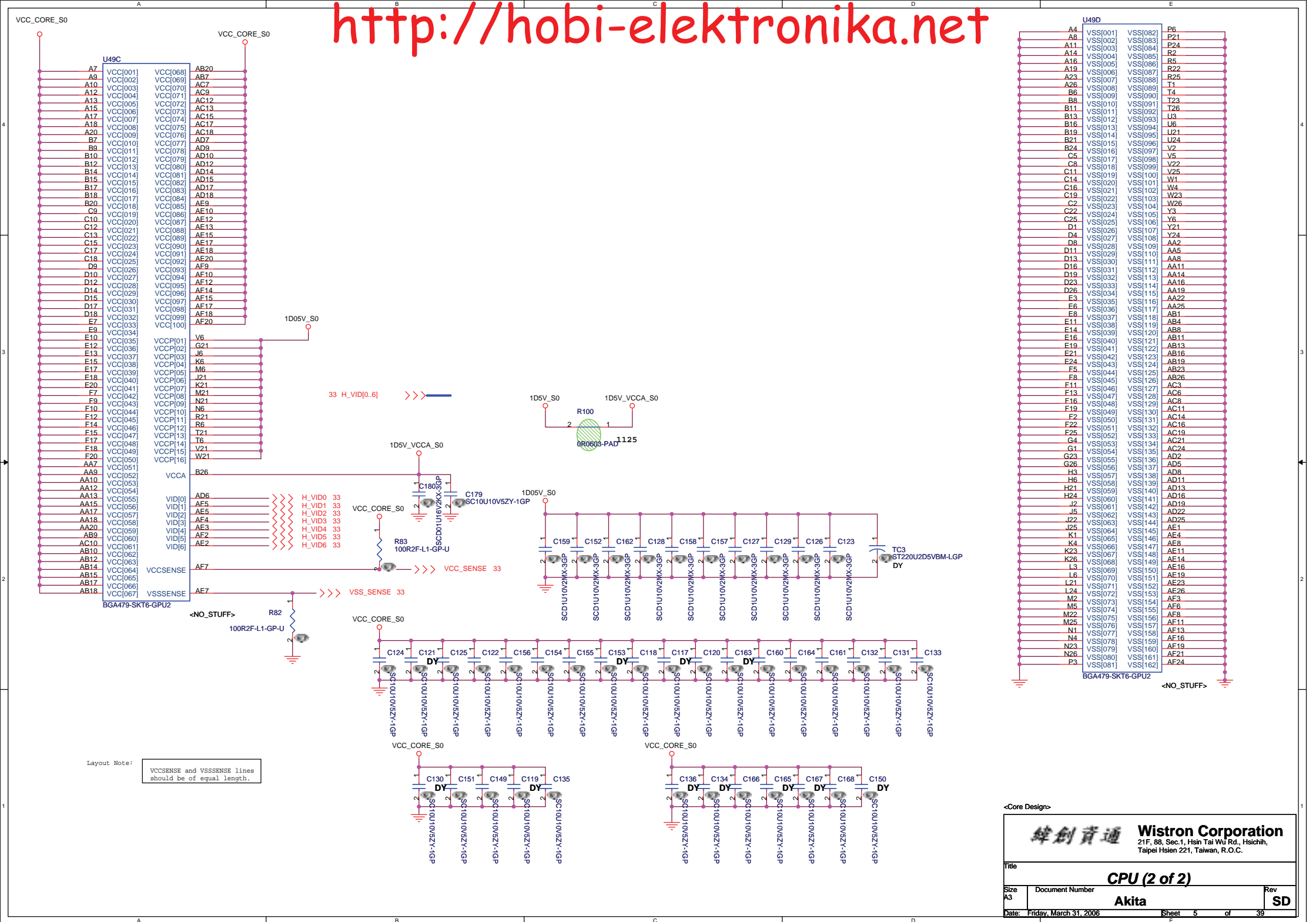
ITP

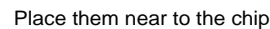
Size A3 Document Number Akita Rev SD

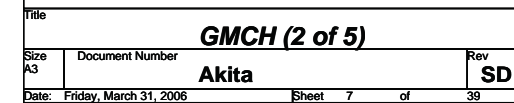
Date: Friday, March 31, 2006 Sheet 2 of 39

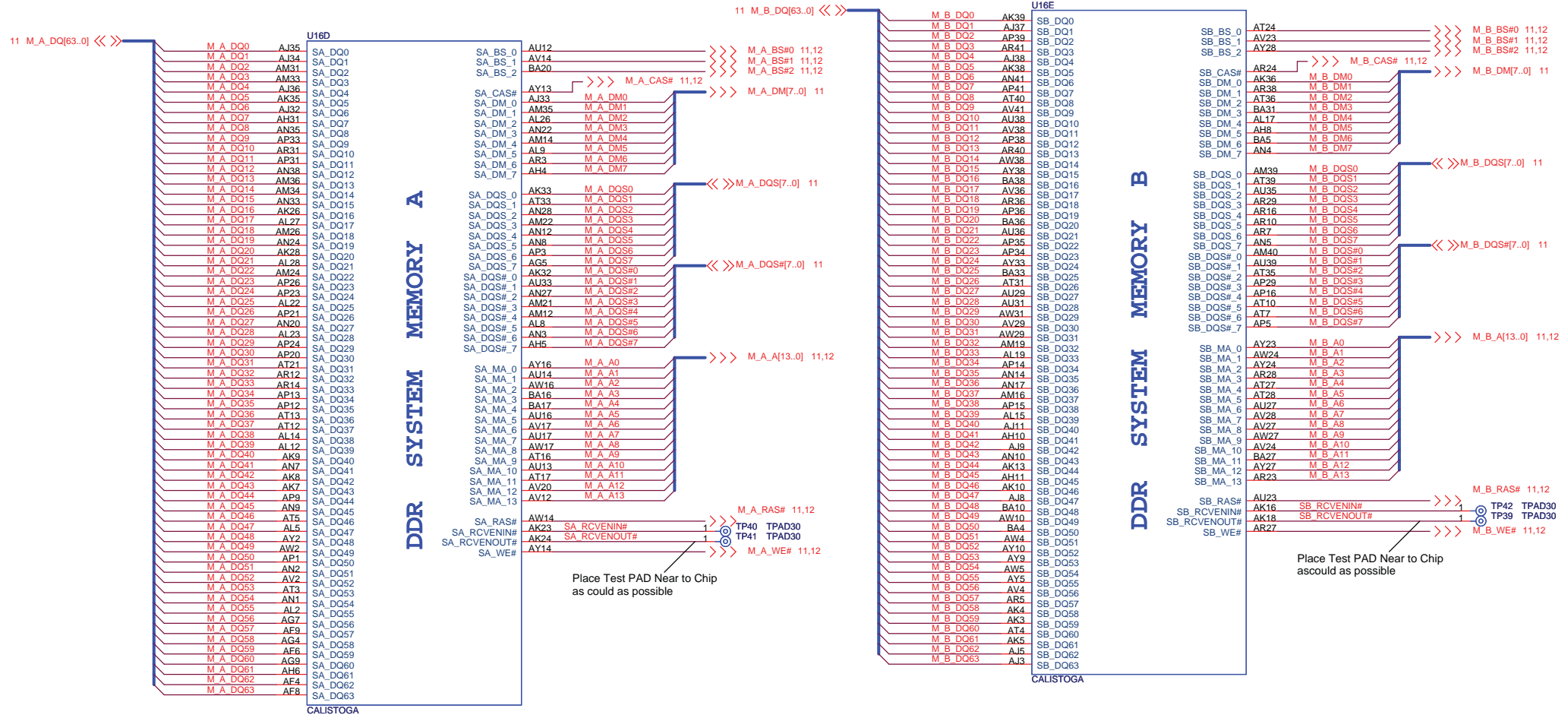




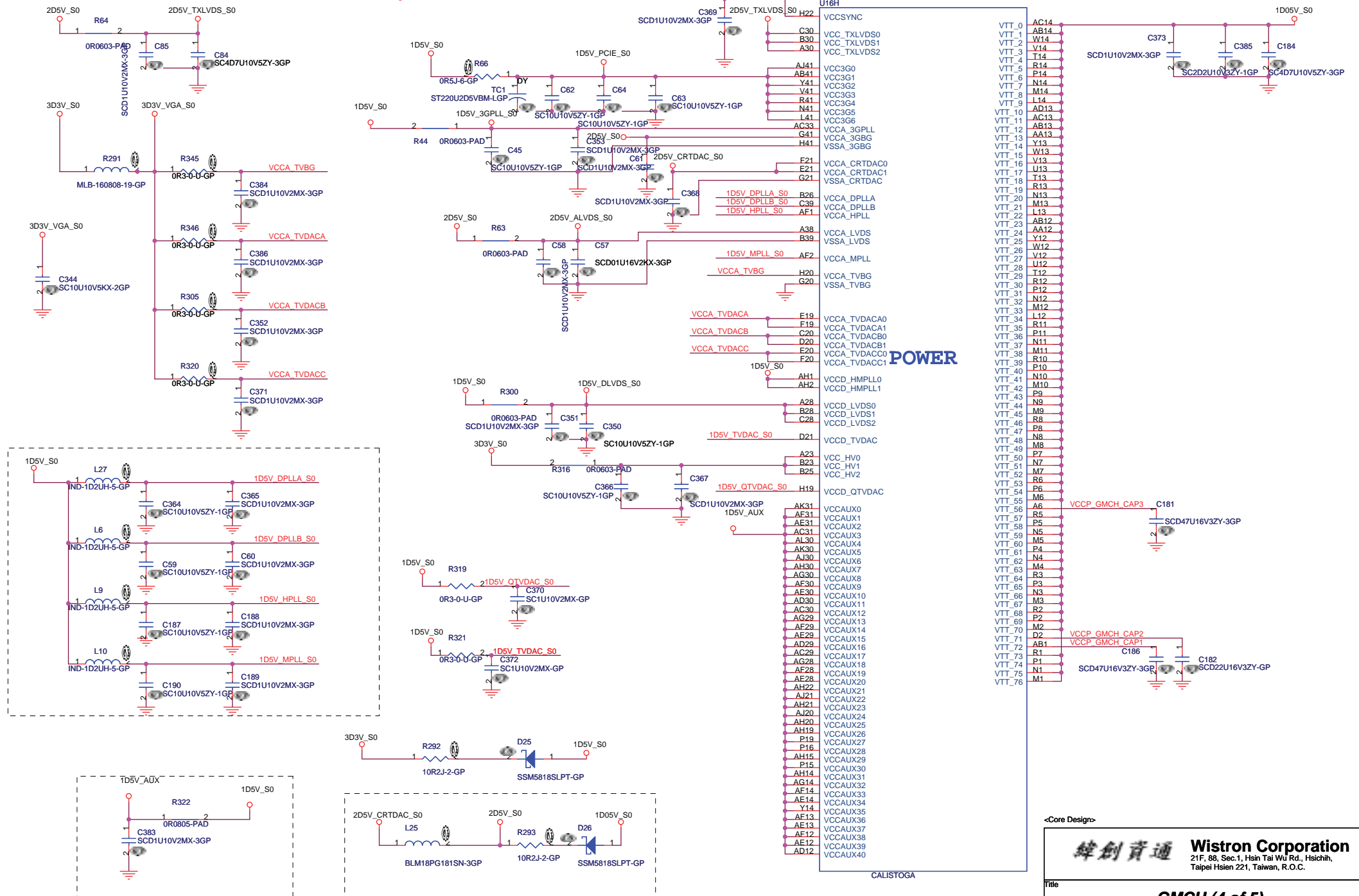


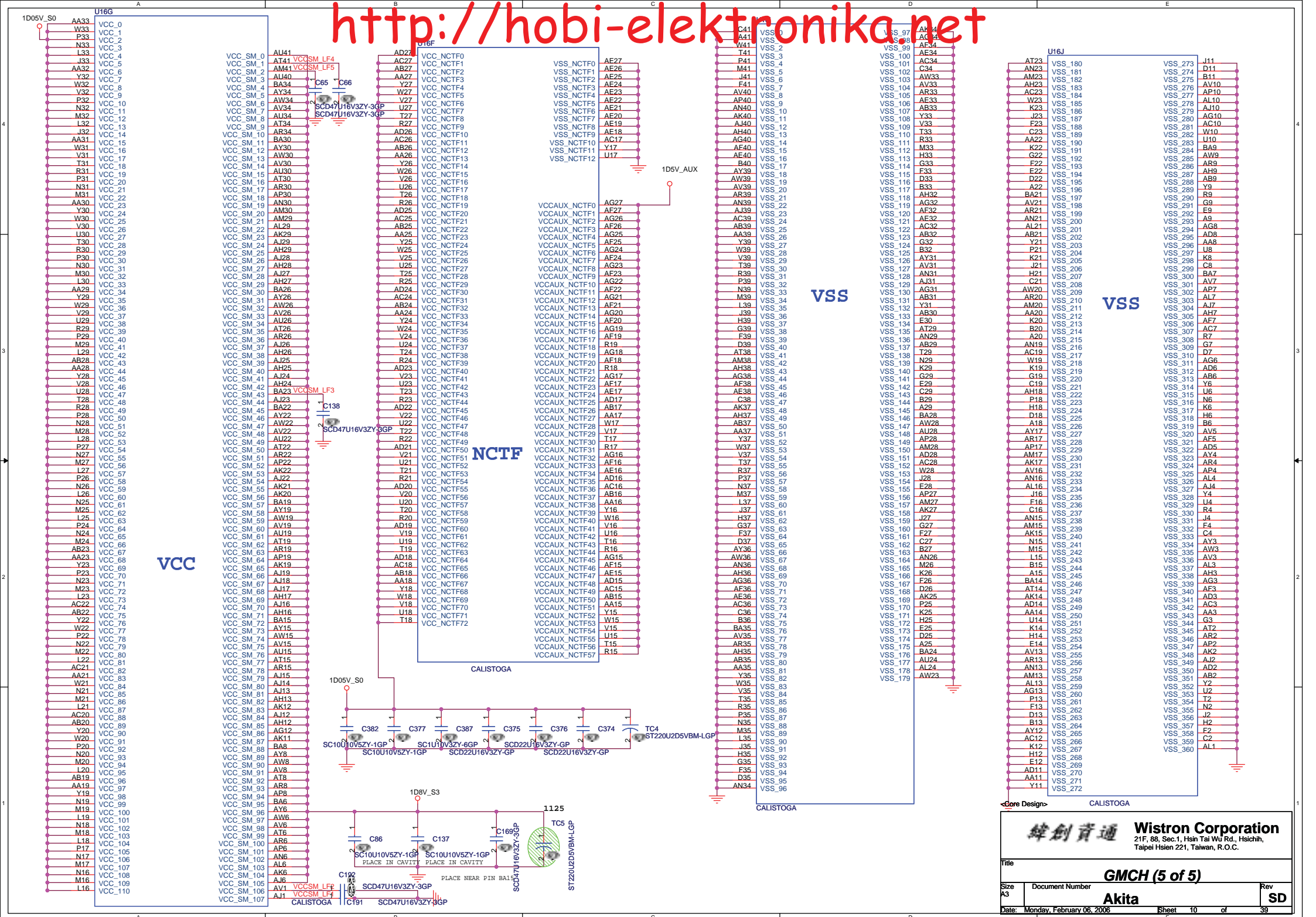






<Core Design>





Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

GMCH (5 of 5)
Akita

Rev SD

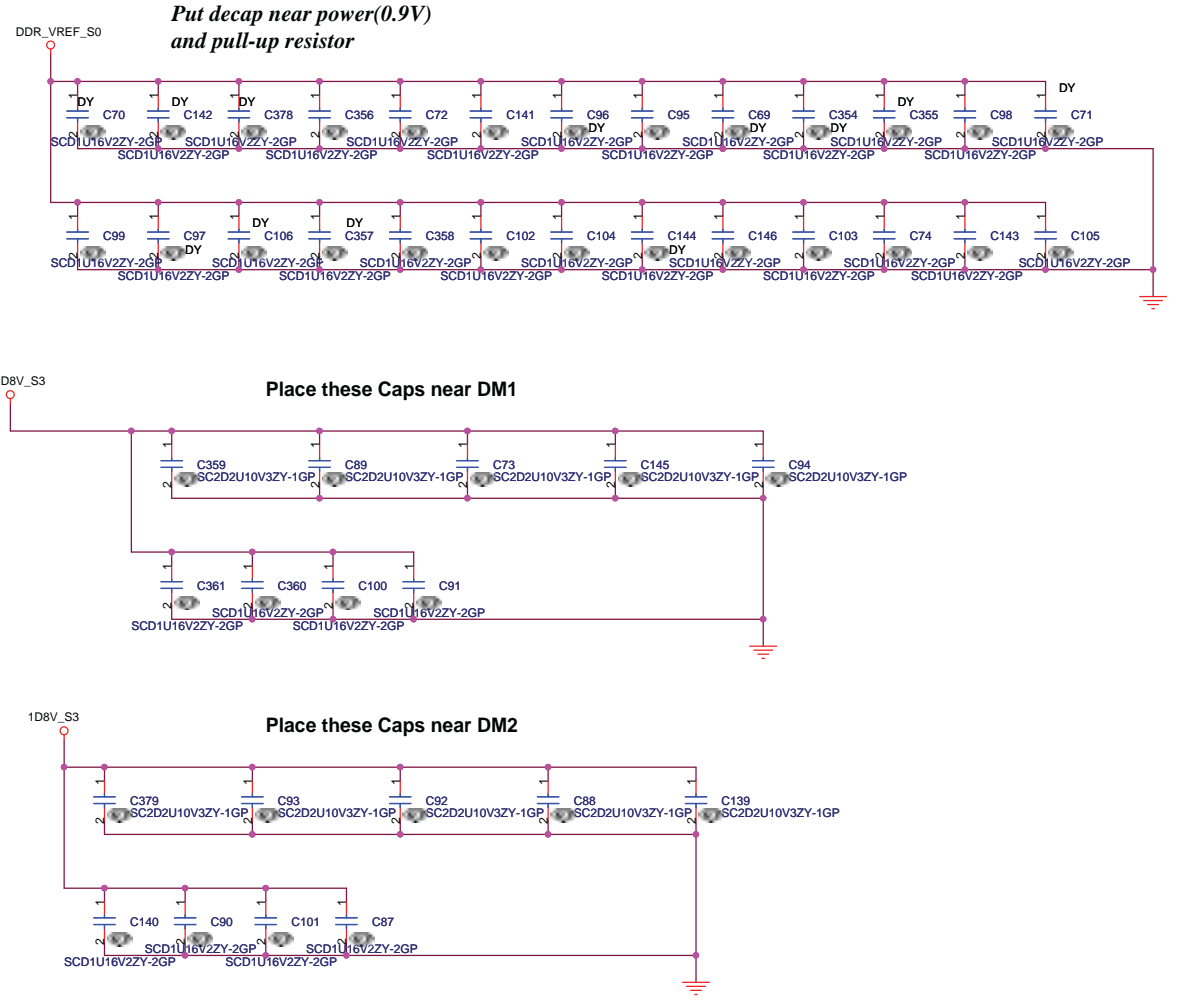
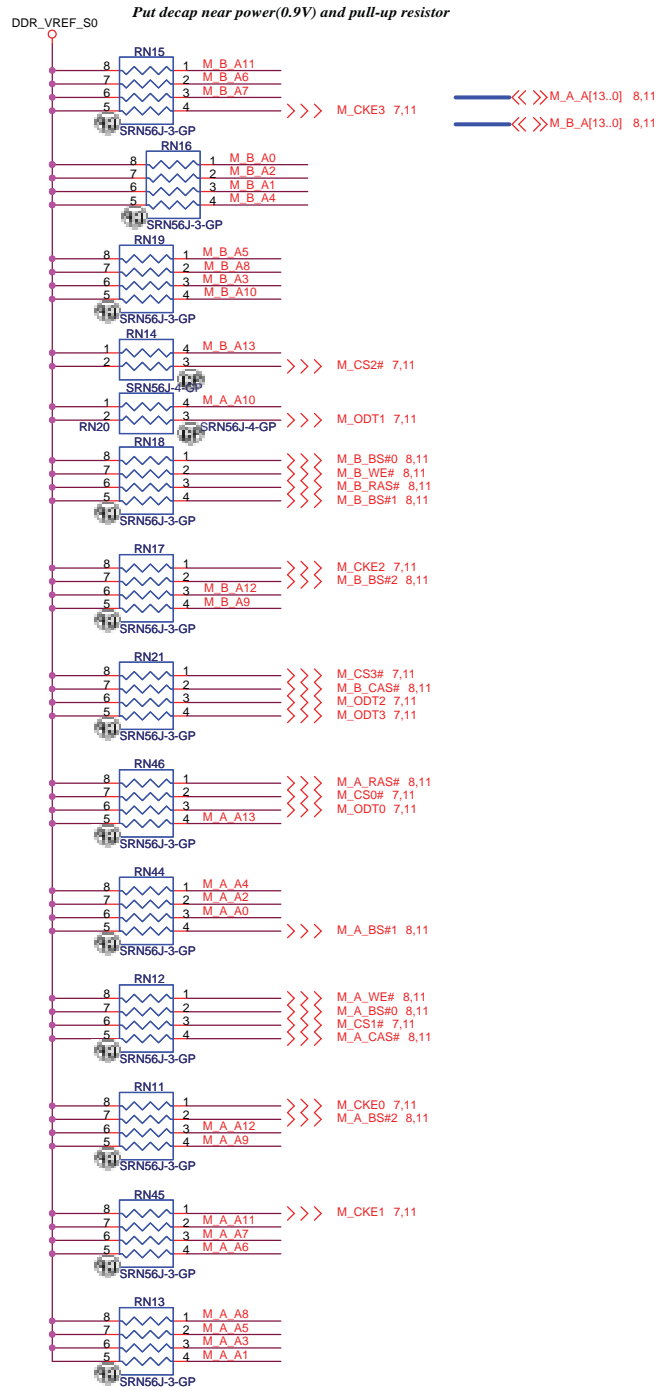
Date: Monday, February 06, 2006 Sheet 10 of 39



Title			
DDR2 Socket			
Size	Document Number		Rev
Custom	Akita		SI
Date: Monday, February 06, 2006		Sheet 11 of	39

PARALLEL TERMINATION

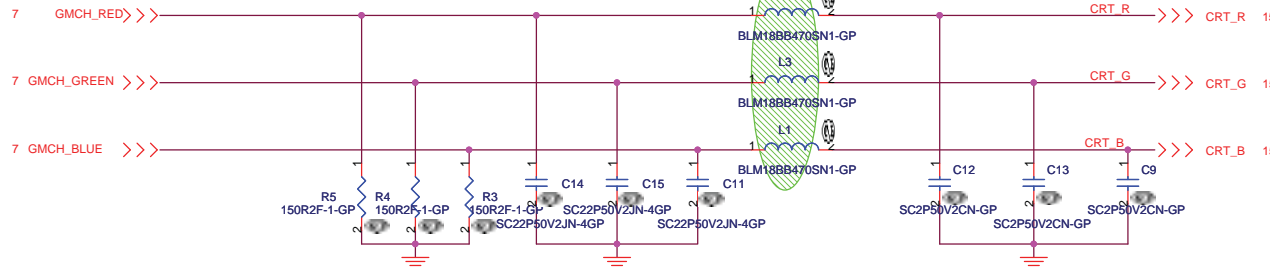
Decoupling Capacitor



CRT I/F & CONNECTOR

<http://hobi-elektronika.net>

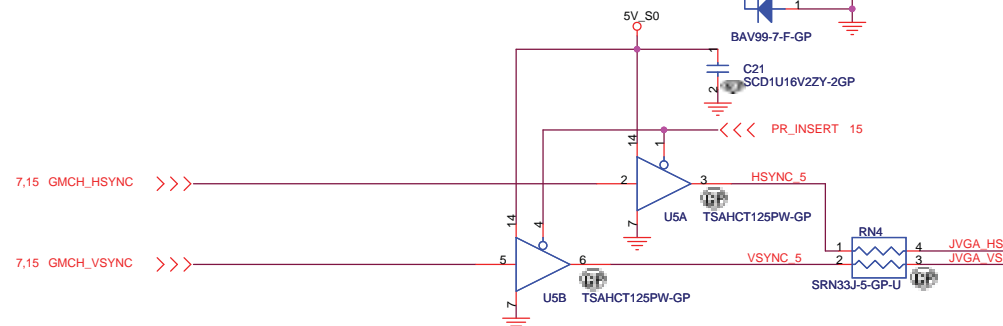
Layout Note:
Place these resistors
close to the CRT-out
connector



Layout Note:

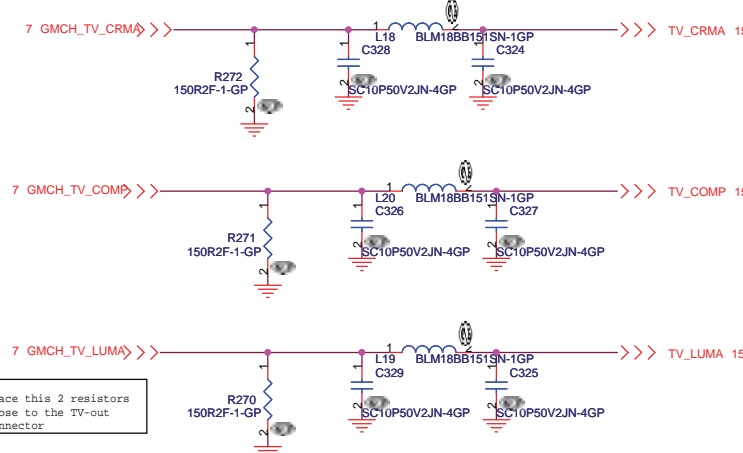
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

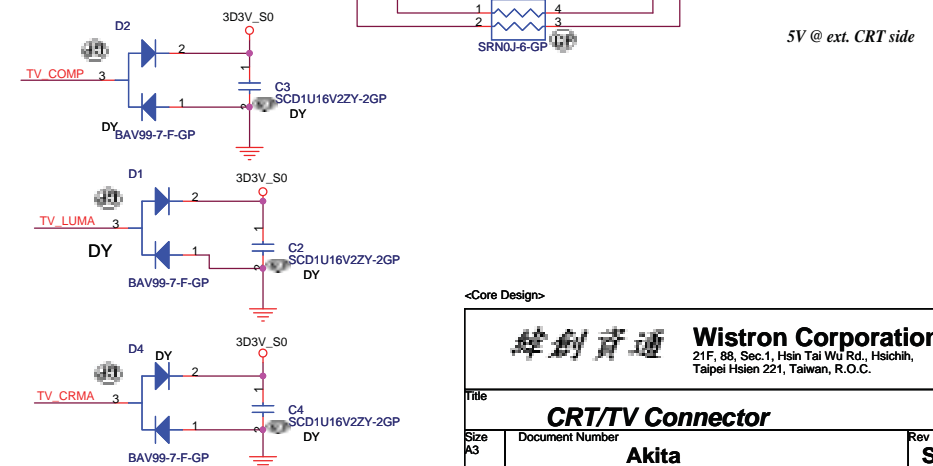
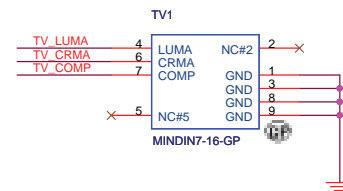


TV OUT CONN

connector



Place this 2 resistors
close to the TV-out
connector



5V @ ext. CRT side

<Core Design>

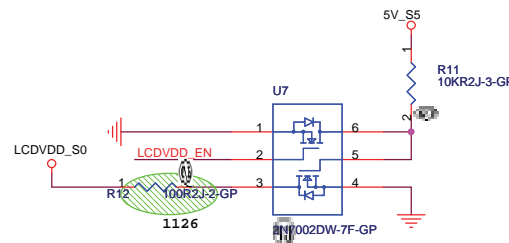
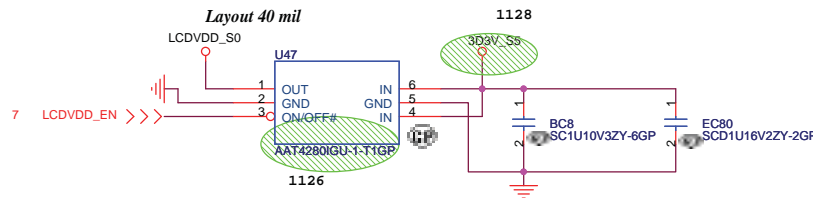
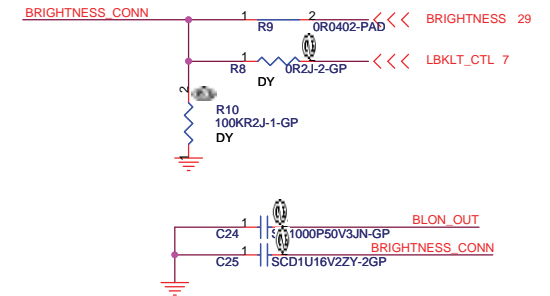
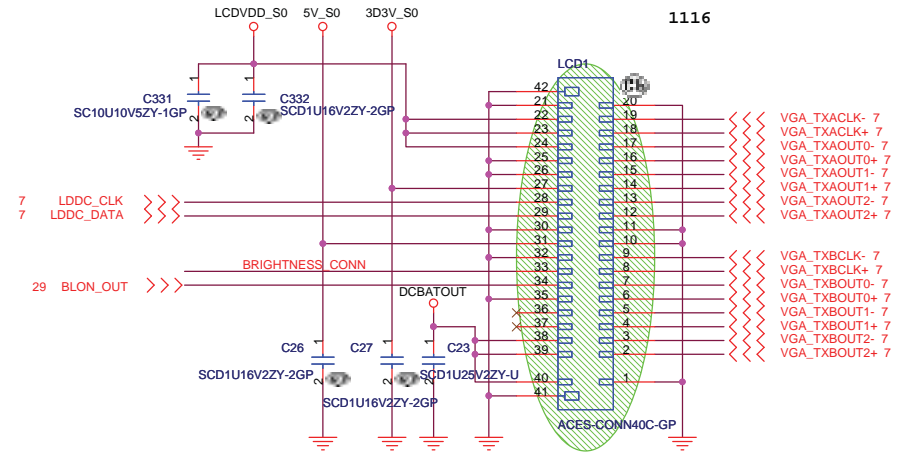
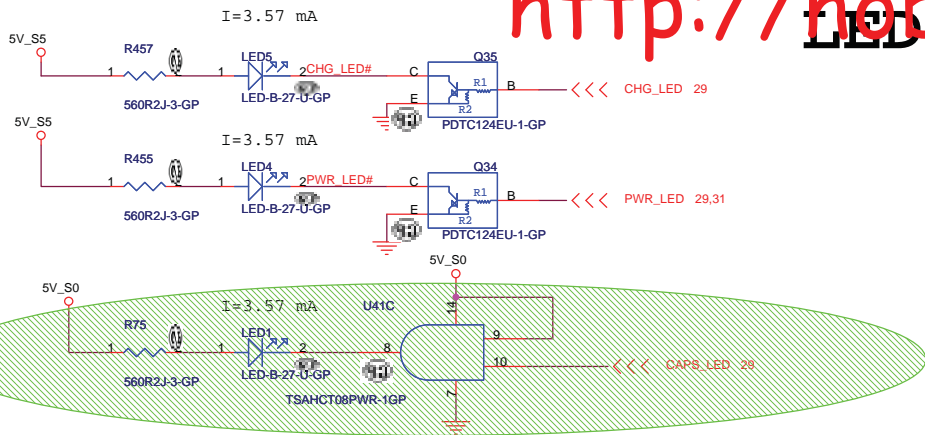
緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CRT/TV Connector			
Size	Document Number	Rev	
A3	Akita	SD	
Date:	Saturday, April 01, 2006	Sheet	13 of 39

LCD/INV CONN

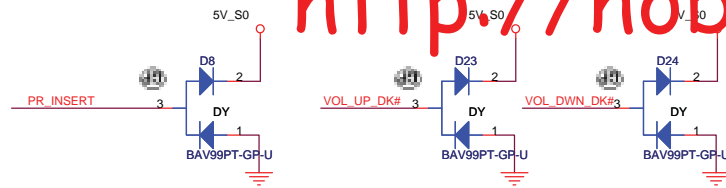


<Core Design>

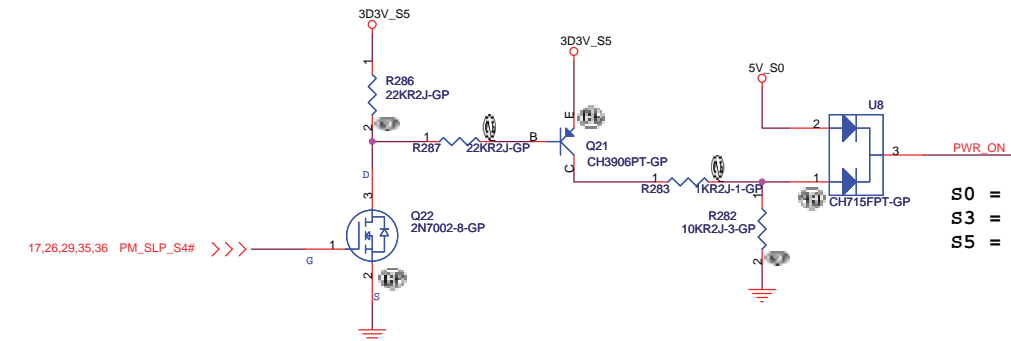
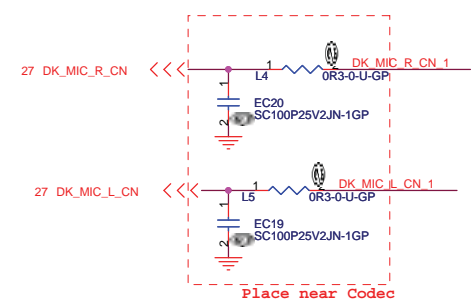
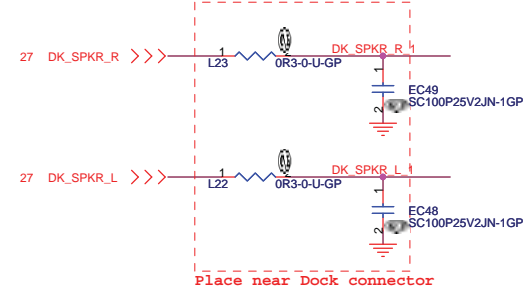
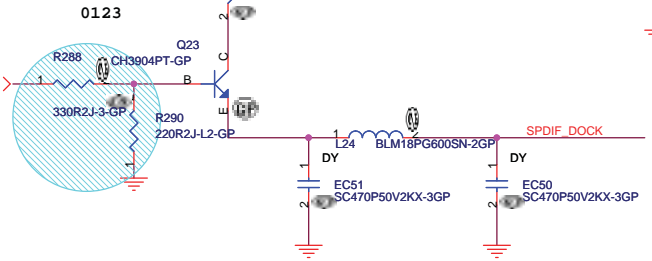
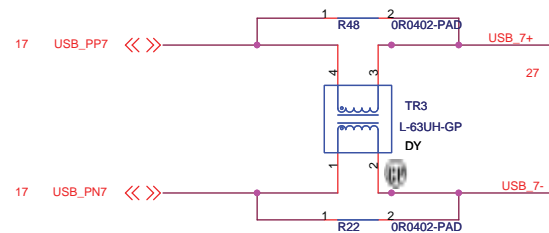
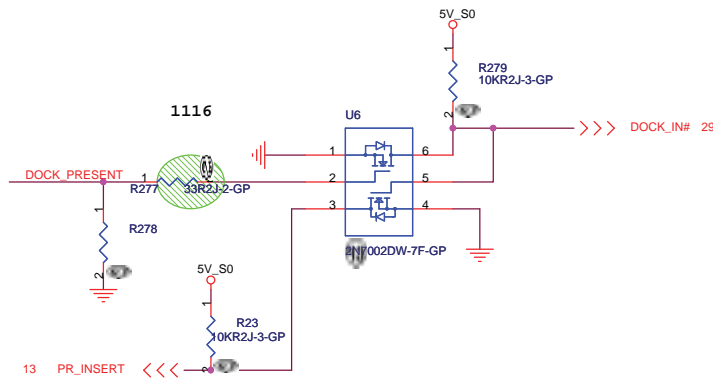
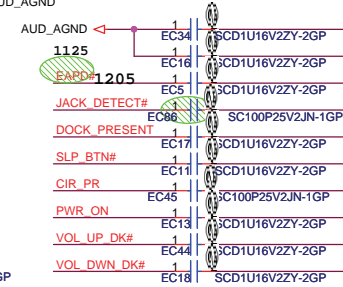
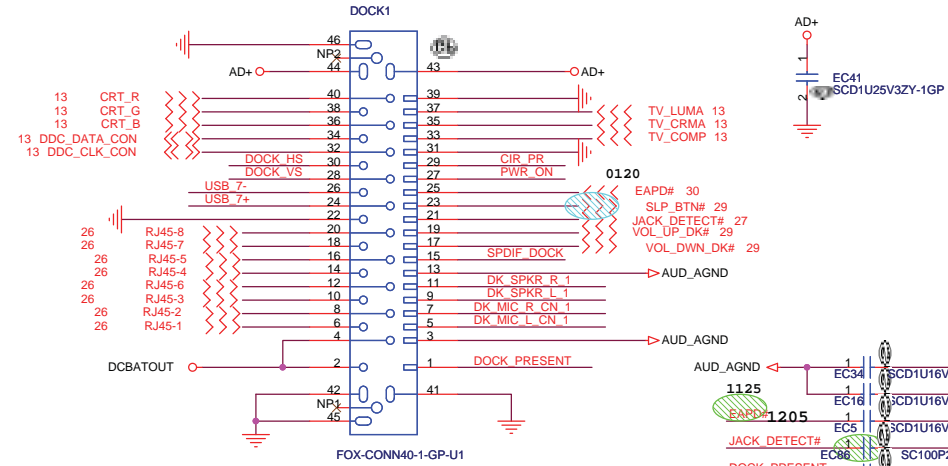
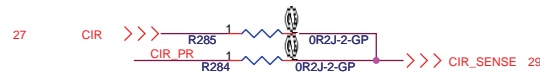
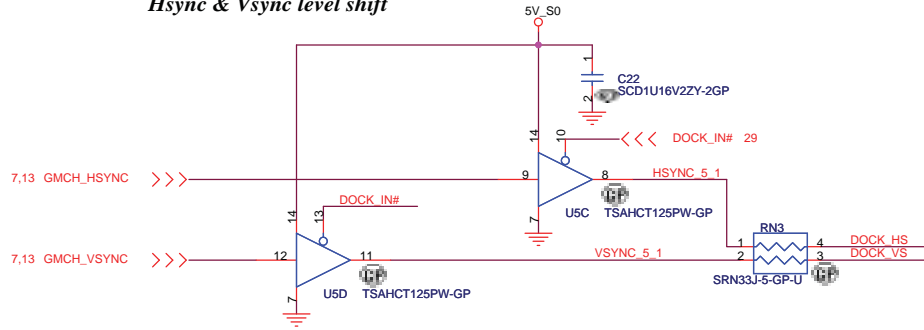
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

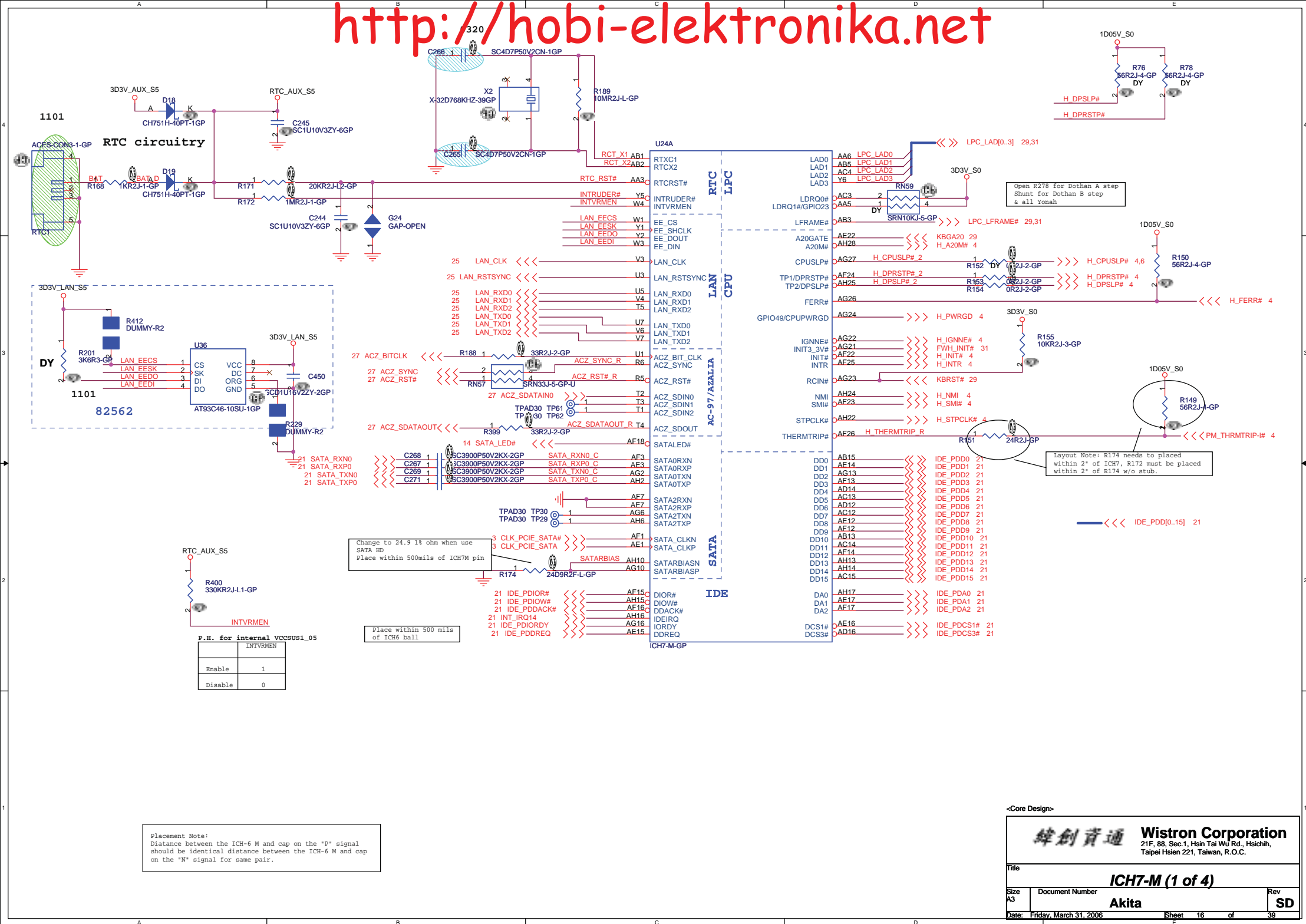
Title			Rev
LCD/Inverter Connector			SD
Size	Document Number	Akita	
Custom			
Date:	Saturday, April 01, 2006	Sheet	14 of 39

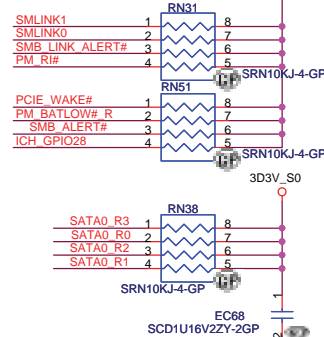
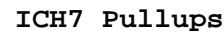


Hsync & Vsync level shift

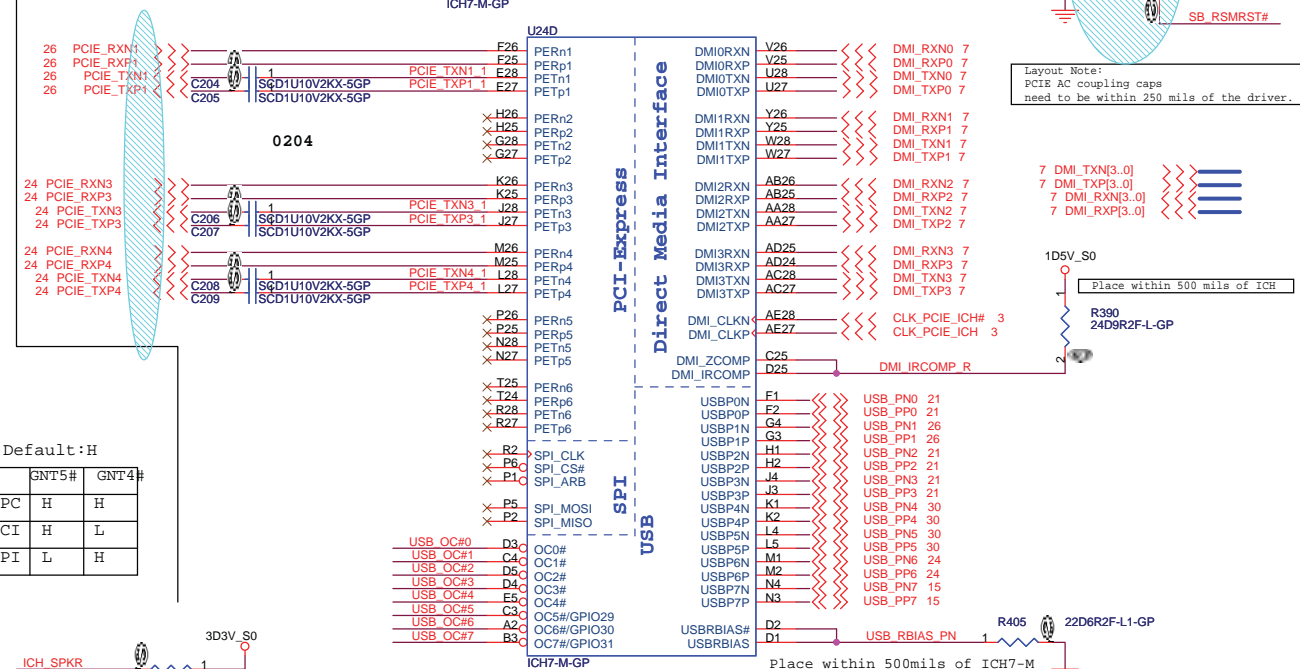
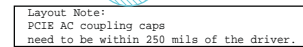


S0 = 4V
S3 = 2.5V
S5 = 0V



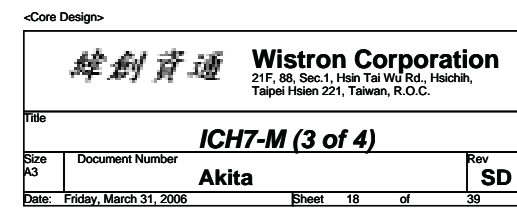


	GNT5#	GNT4#
LPC	H	H
PCI	H	L
SPI	L	H

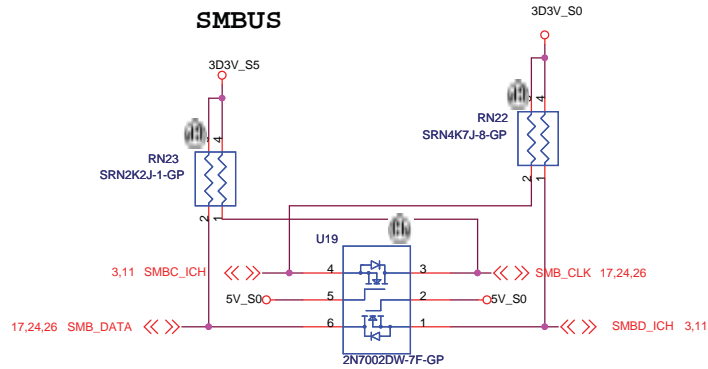


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
ICH7-M (2 of 4)			
Size A3	Document Number		Rev
	Akita		SD
Date:	Friday, March 31, 2006		Sheet 17 of 39

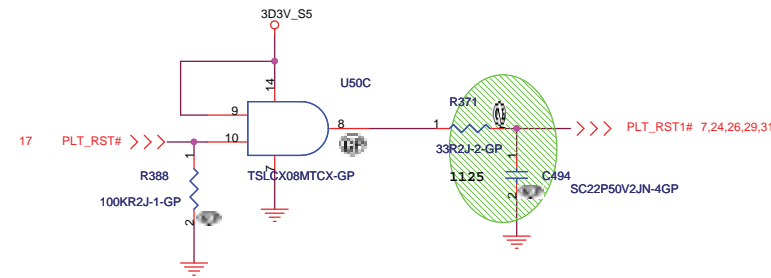
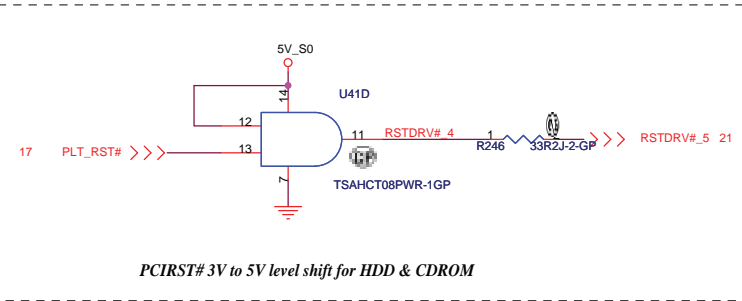
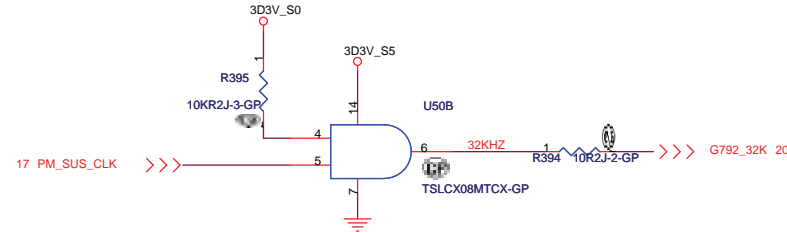


SMBUS

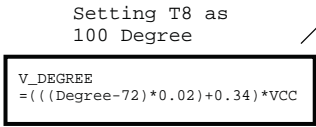


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

32K suspend clock output

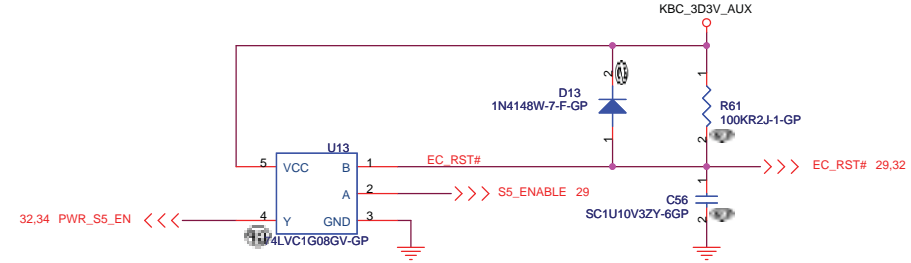


U24E		
A4	VSS[1]	VSS[98]
A23	VSS[2]	VSS[99]
B1	VSS[3]	VSS[100]
B8	VSS[4]	VSS[101]
B11	VSS[5]	VSS[102]
B14	VSS[6]	VSS[103]
B17	VSS[7]	VSS[104]
B20	VSS[8]	VSS[105]
B28	VSS[9]	VSS[106]
C2	VSS[10]	VSS[107]
C6	VSS[11]	VSS[108]
C27	VSS[12]	VSS[109]
D10	VSS[13]	VSS[110]
D13	VSS[14]	VSS[111]
D18	VSS[15]	VSS[112]
D21	VSS[16]	VSS[113]
D24	VSS[17]	VSS[114]
E1	VSS[18]	VSS[115]
E2	VSS[19]	VSS[116]
E4	VSS[20]	VSS[117]
E8	VSS[21]	VSS[118]
E15	VSS[22]	VSS[119]
F3	VSS[23]	VSS[120]
F4	VSS[24]	VSS[121]
F5	VSS[25]	VSS[122]
F12	VSS[26]	VSS[123]
F27	VSS[27]	VSS[124]
F28	VSS[28]	VSS[125]
G1	VSS[29]	VSS[126]
G2	VSS[30]	VSS[127]
G5	VSS[31]	VSS[128]
G6	VSS[32]	VSS[129]
G9	VSS[33]	VSS[130]
G14	VSS[34]	VSS[131]
G18	VSS[35]	VSS[132]
G21	VSS[36]	VSS[133]
G24	VSS[37]	VSS[134]
G25	VSS[38]	VSS[135]
G26	VSS[39]	VSS[136]
H3	VSS[40]	VSS[137]
H4	VSS[41]	VSS[138]
H5	VSS[42]	VSS[139]
H24	VSS[43]	VSS[140]
H27	VSS[44]	VSS[141]
H28	VSS[45]	VSS[142]
J1	VSS[46]	VSS[143]
J2	VSS[47]	VSS[144]
J5	VSS[48]	VSS[145]
J24	VSS[49]	VSS[146]
J25	VSS[50]	VSS[147]
J26	VSS[51]	VSS[148]
K24	VSS[52]	VSS[149]
K27	VSS[53]	VSS[150]
K28	VSS[54]	VSS[151]
L13	VSS[55]	VSS[152]
L15	VSS[56]	VSS[153]
L24	VSS[57]	VSS[154]
L25	VSS[58]	VSS[155]
L26	VSS[59]	VSS[156]
M3	VSS[60]	VSS[157]
M4	VSS[61]	VSS[158]
M5	VSS[62]	VSS[159]
M12	VSS[63]	VSS[160]
M13	VSS[64]	VSS[161]
M14	VSS[65]	VSS[162]
M15	VSS[66]	VSS[163]
M16	VSS[67]	VSS[164]
M17	VSS[68]	VSS[165]
M24	VSS[69]	VSS[166]
M27	VSS[70]	VSS[167]
M28	VSS[71]	VSS[168]
N1	VSS[72]	VSS[169]
N2	VSS[73]	VSS[170]
N5	VSS[74]	VSS[171]
N6	VSS[75]	VSS[172]
N11	VSS[76]	VSS[173]
N12	VSS[77]	VSS[174]
N13	VSS[78]	VSS[175]
N14	VSS[79]	VSS[176]
N15	VSS[80]	VSS[177]
N16	VSS[81]	VSS[178]
N17	VSS[82]	VSS[179]
N18	VSS[83]	VSS[180]
N24	VSS[84]	VSS[181]
N25	VSS[85]	VSS[182]
N28	VSS[86]	VSS[183]
P3	VSS[87]	VSS[184]
P4	VSS[88]	VSS[185]
P12	VSS[89]	VSS[186]
P13	VSS[90]	VSS[187]
P14	VSS[91]	VSS[188]
P15	VSS[92]	VSS[189]
P16	VSS[93]	VSS[190]
P17	VSS[94]	VSS[191]
P24	VSS[95]	VSS[192]
P27	VSS[96]	VSS[193]
	VSS[97]	VSS[194]



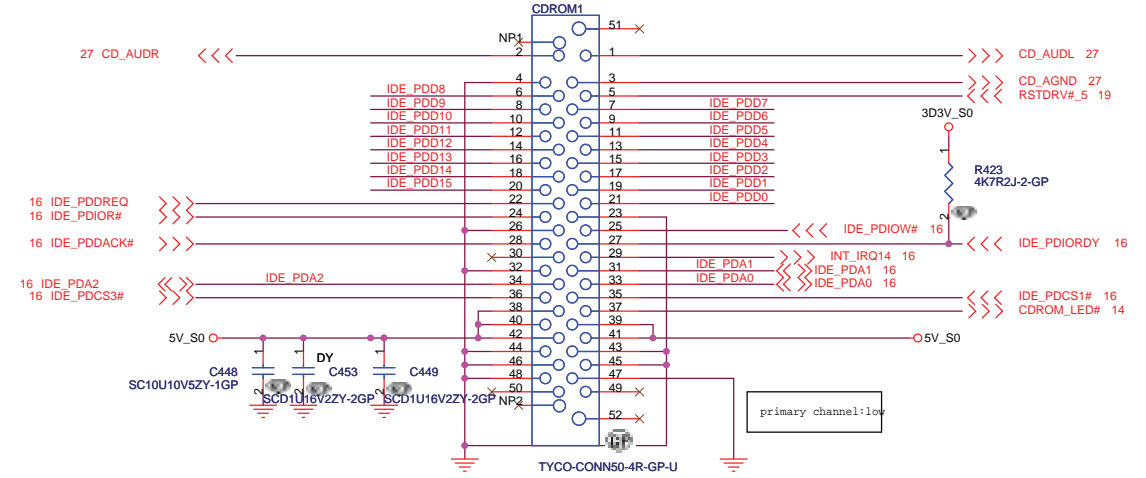
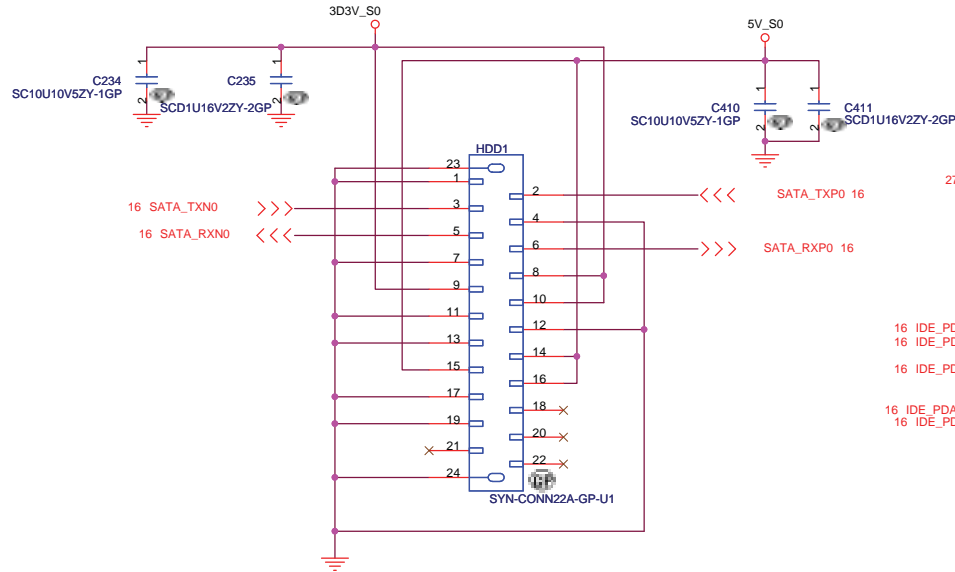
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close
as possible

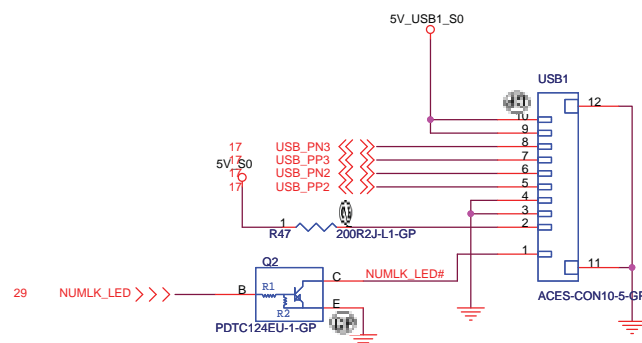
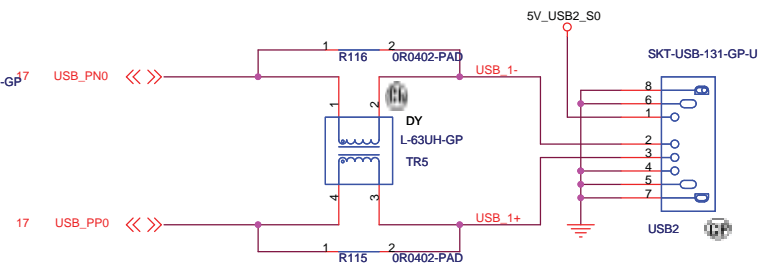
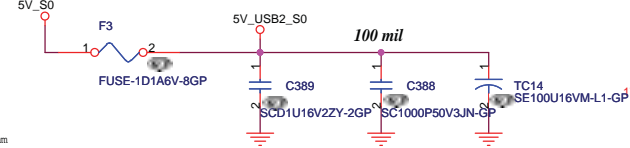
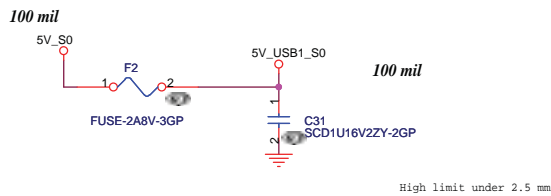


SATA HD Connector

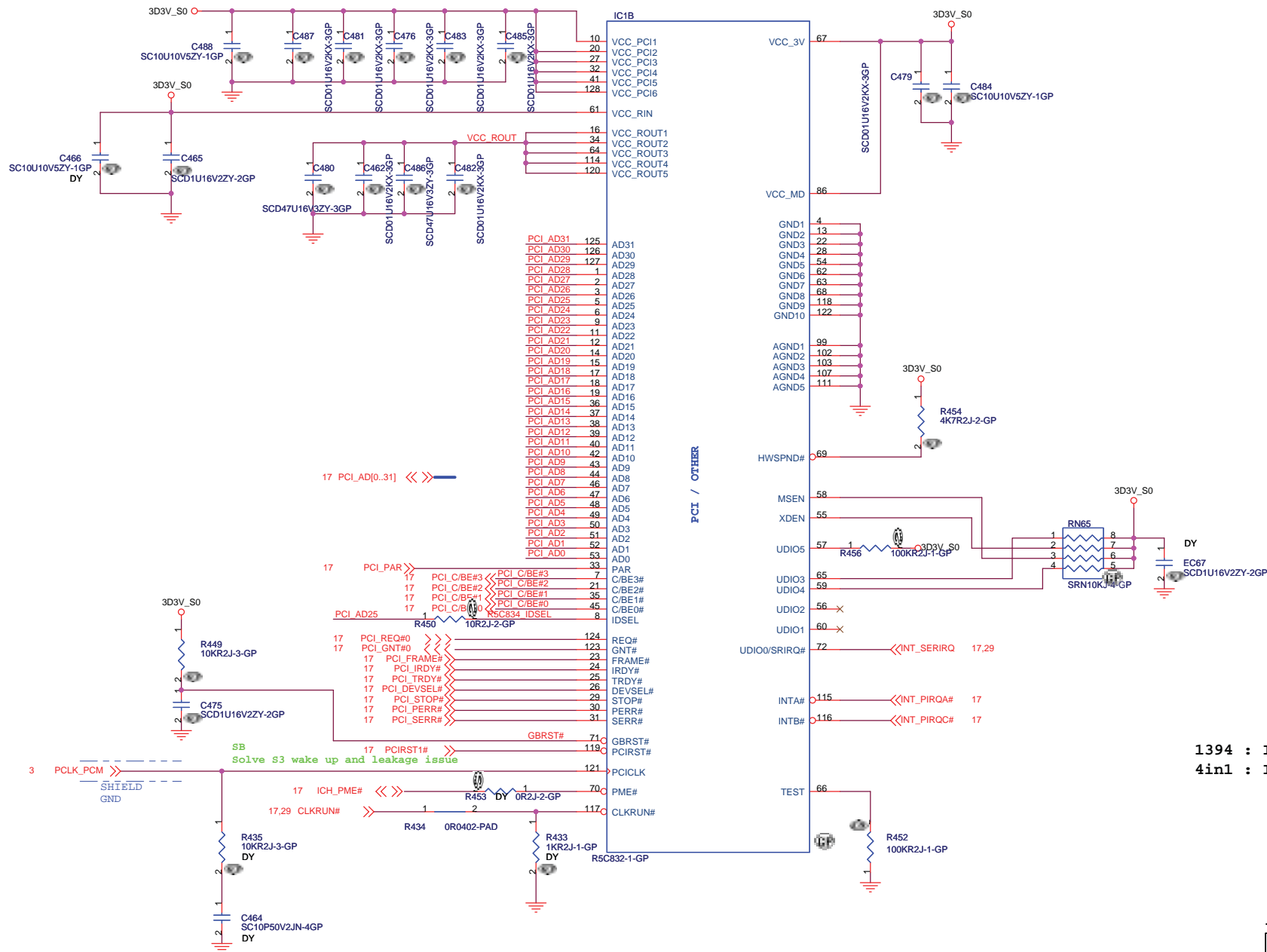
CD-ROM CONNECTOR



USB PORT



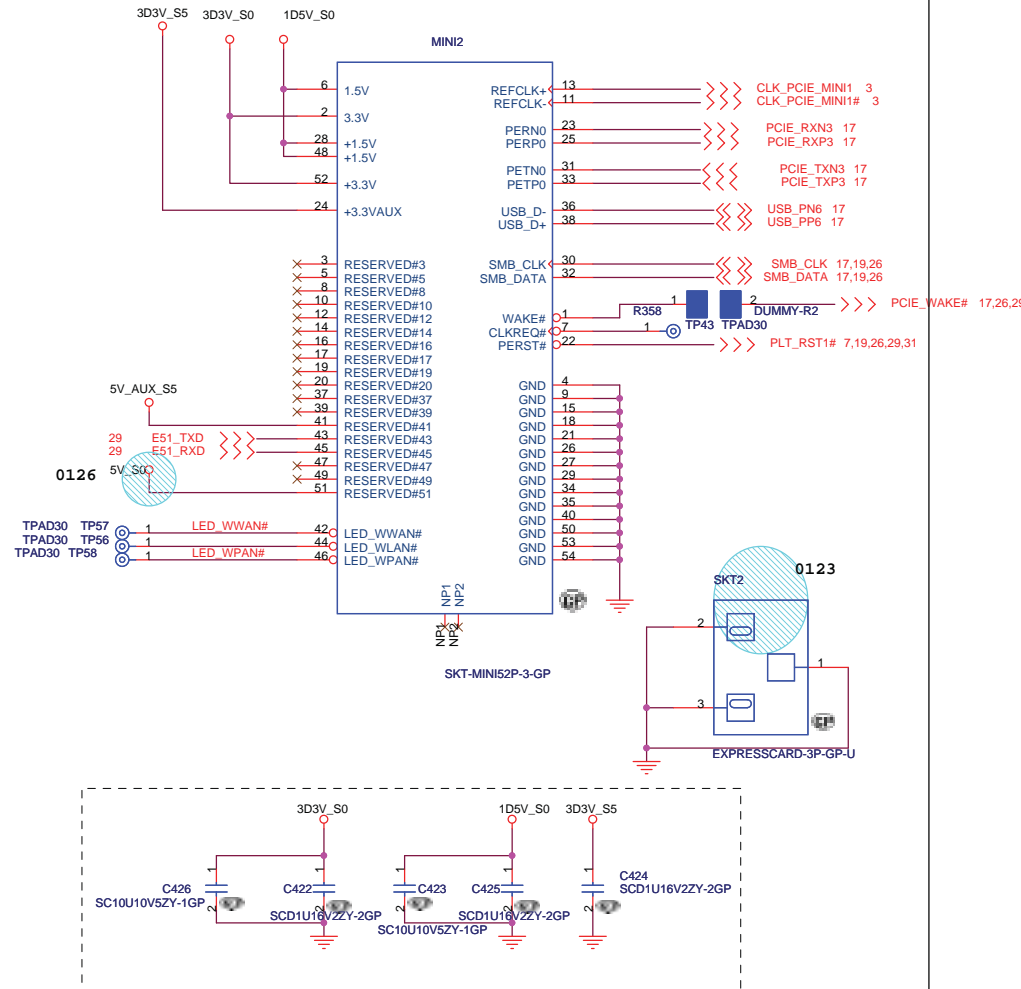
<Core Design>



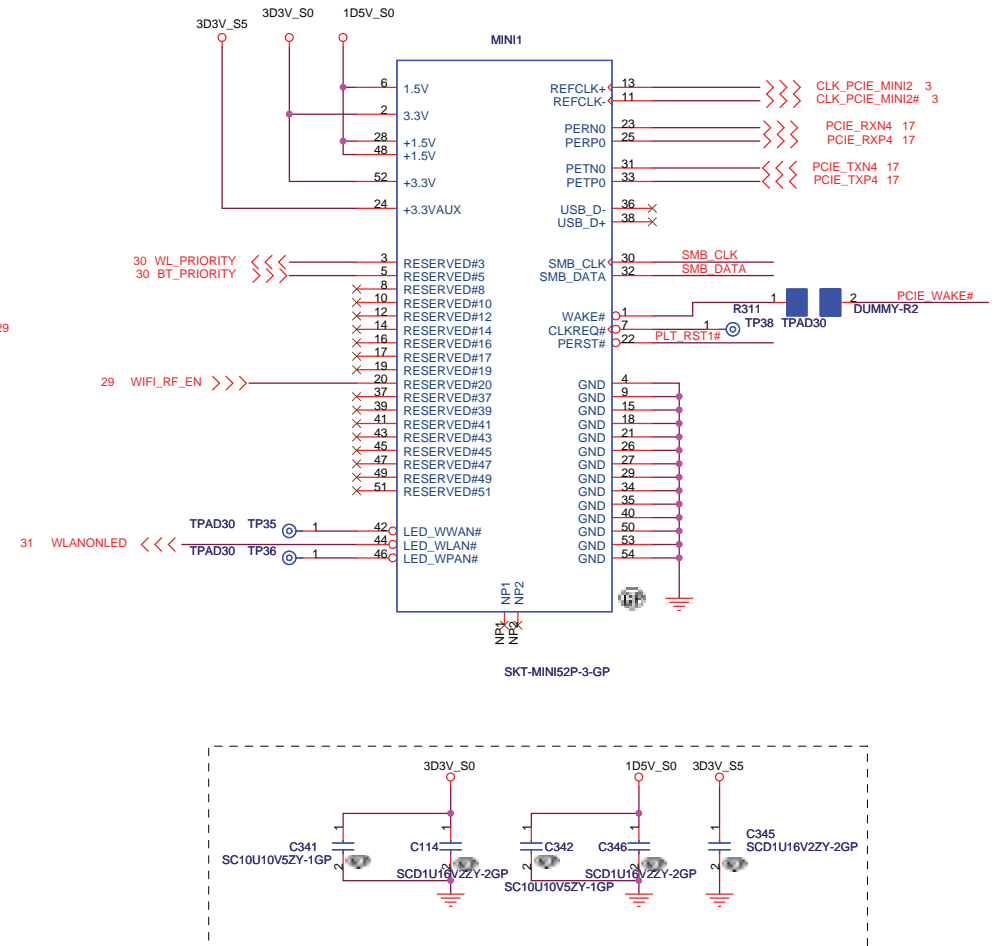
```
1394 : INTA#
4in1  : INTB#
```



Mini Card Connector 1



Mini Card Connector 2

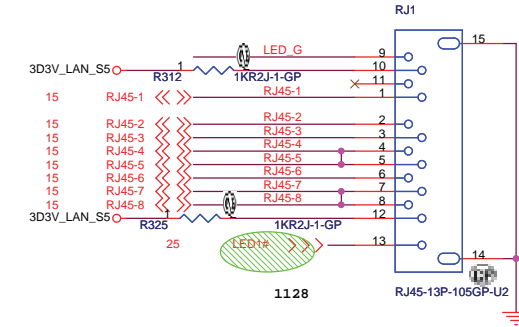
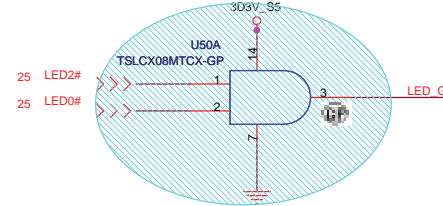
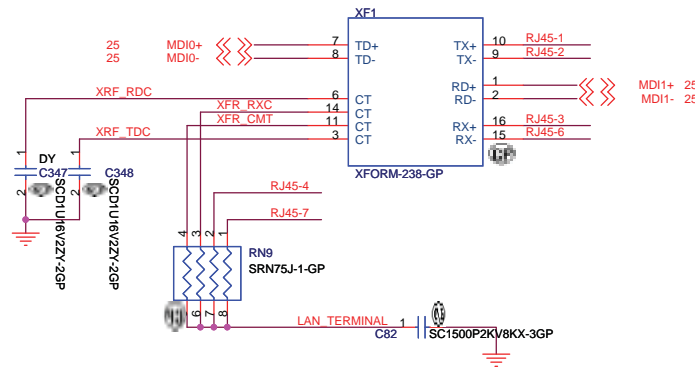


<Core Design>



10/100M Lan Transformer

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



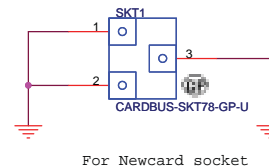
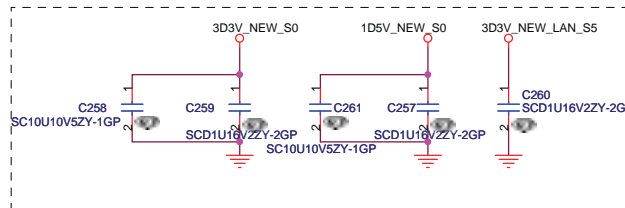
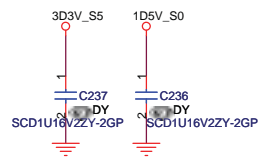
Green : Link up
Blinking : TX/RX activity

PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

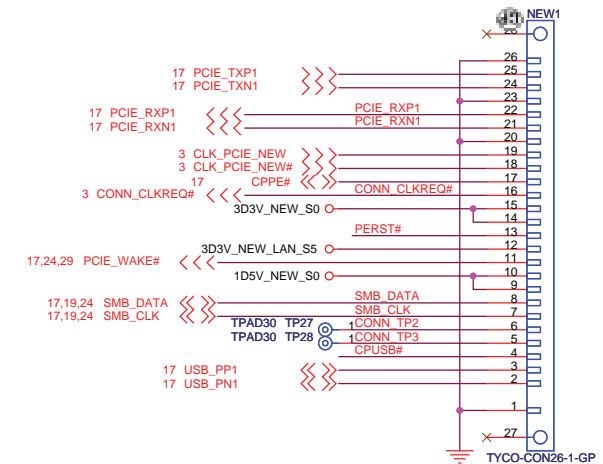
NEWCARD Connector

Place them Near to Chip

Place them Near to Connector

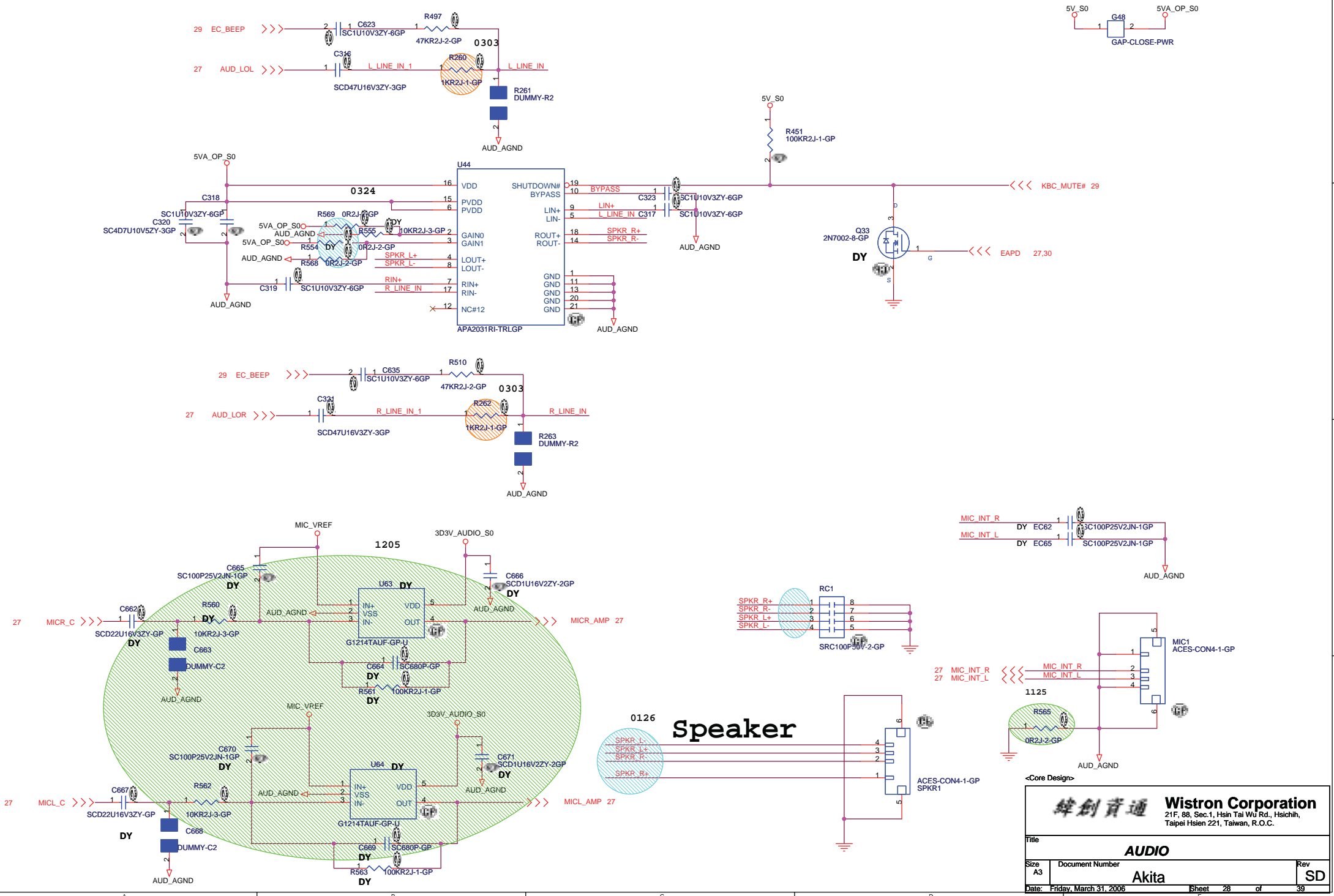


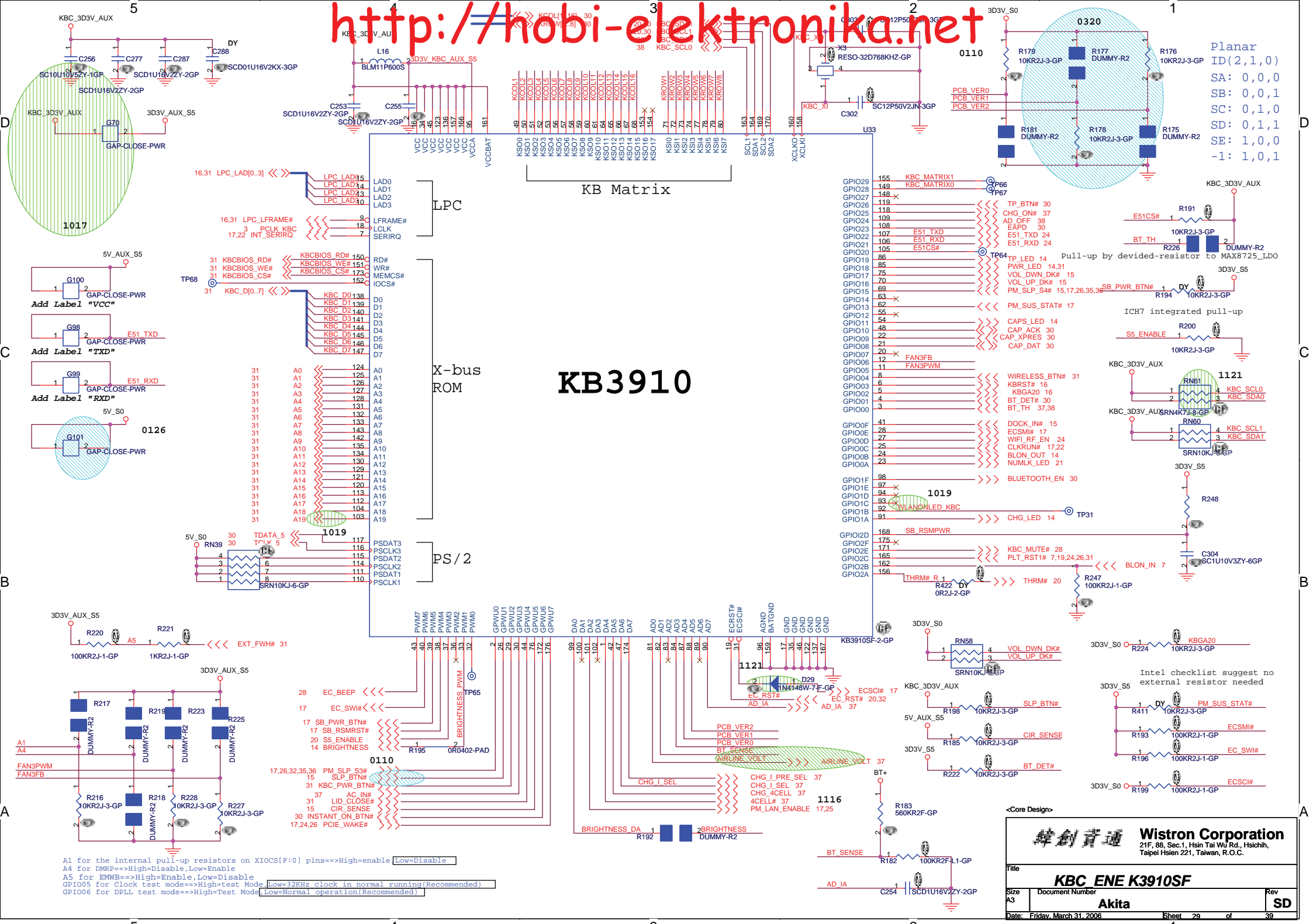
For Newcard socket



<Core Design>







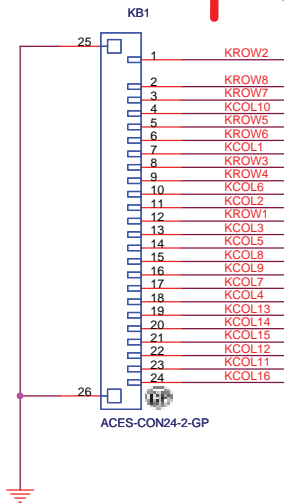
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable Low=Disable
A4 for DMRP==>High=Disable, Low=Enable
A5 for EMWB==>High=Enable, Low=Disable
GPIO05 for Clock test mode==>High=test Mode Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode Low=Normal operation(Recommended)

Internal KeyBoard Connector

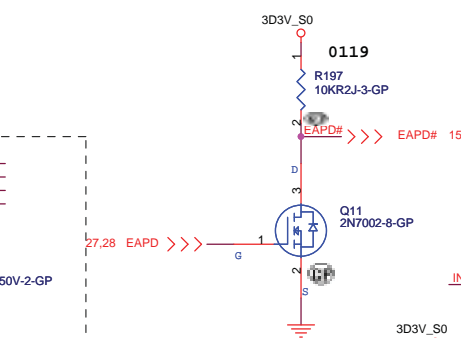
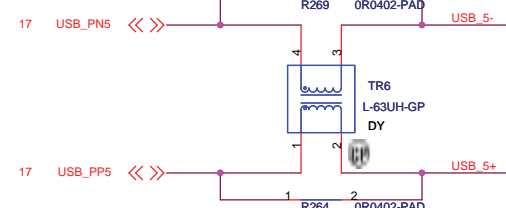
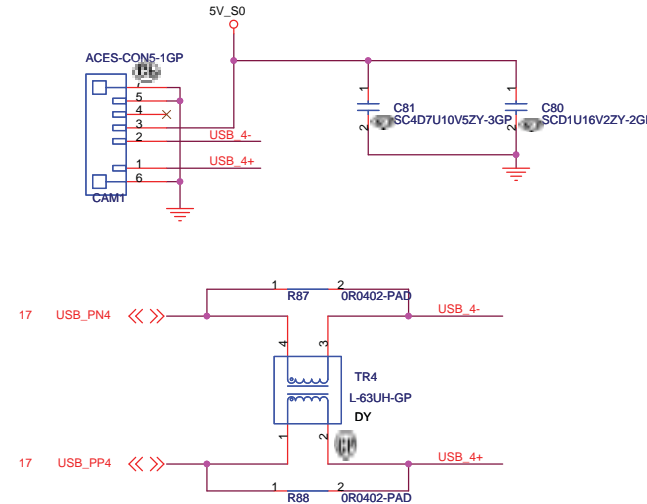
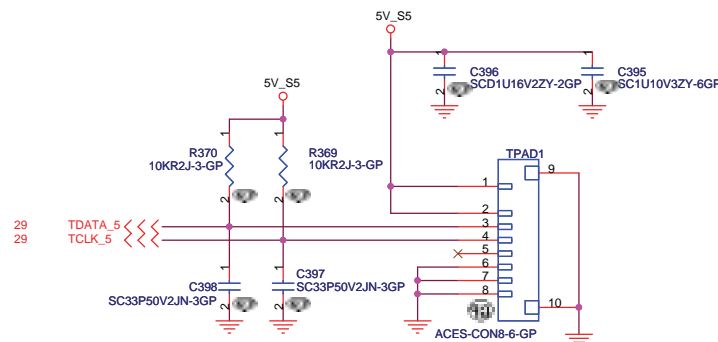
29 KROW[1..8] <<< <<<
29 KCOL[1..16] <<< <<<

Keyboard matrix (from vendor)

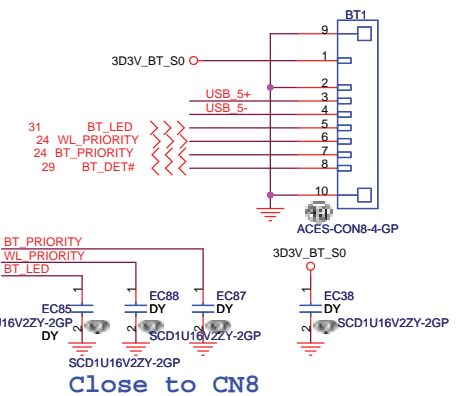
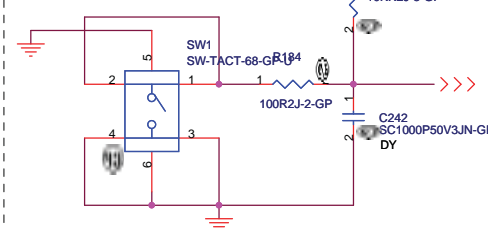
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



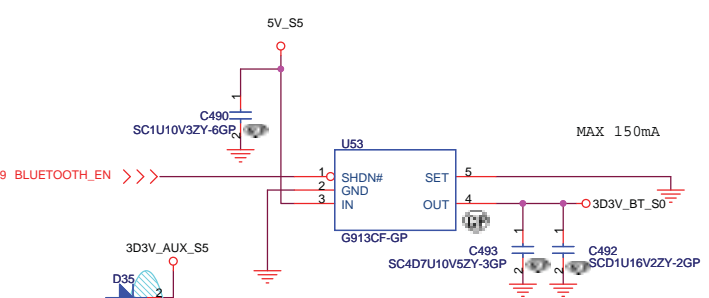
TouchPad Connector



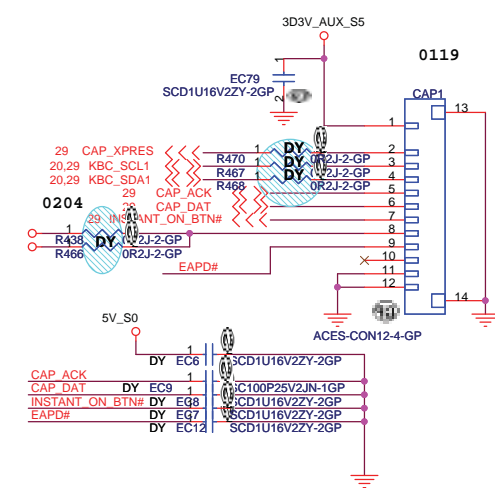
TOUCH-PAD SWITCH



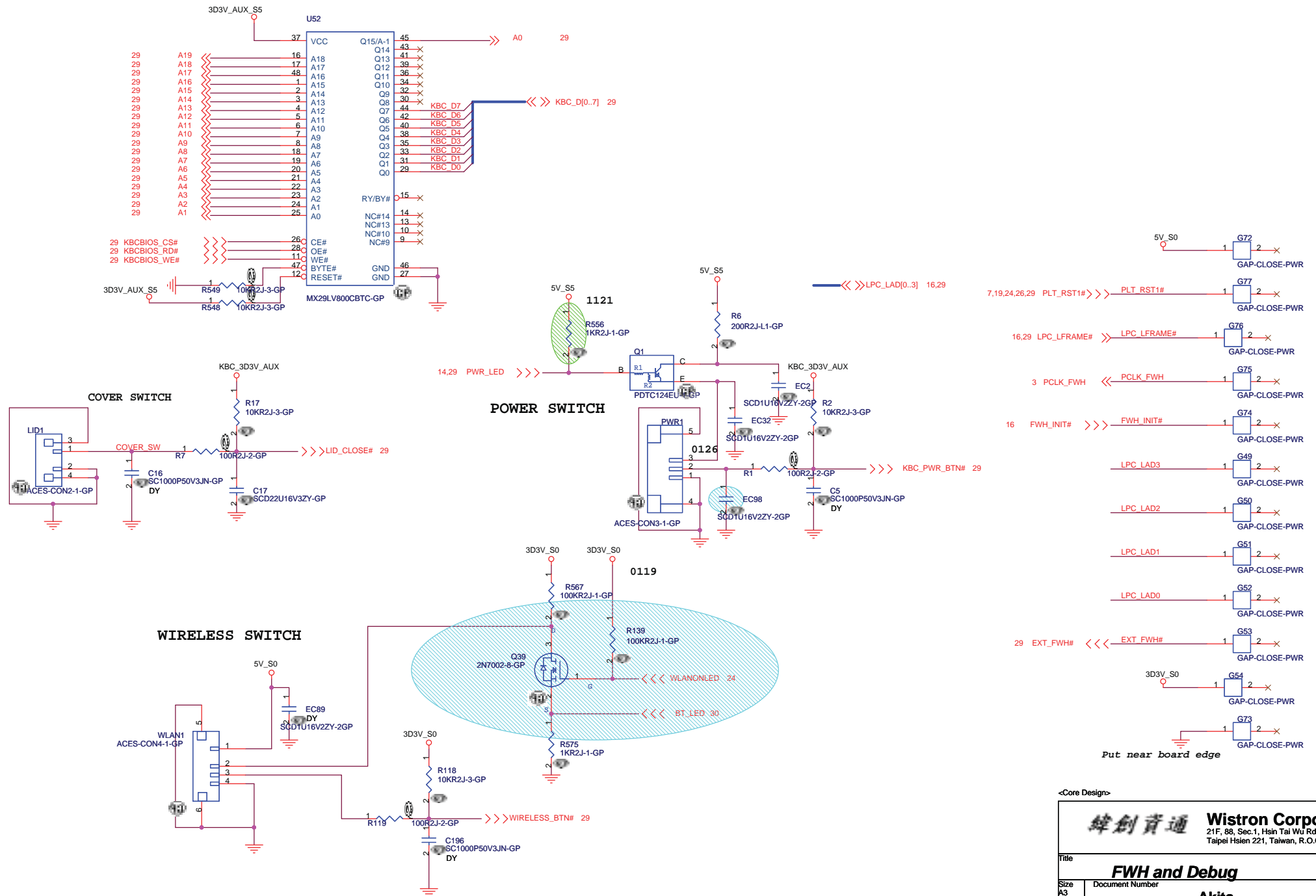
Close to CN8

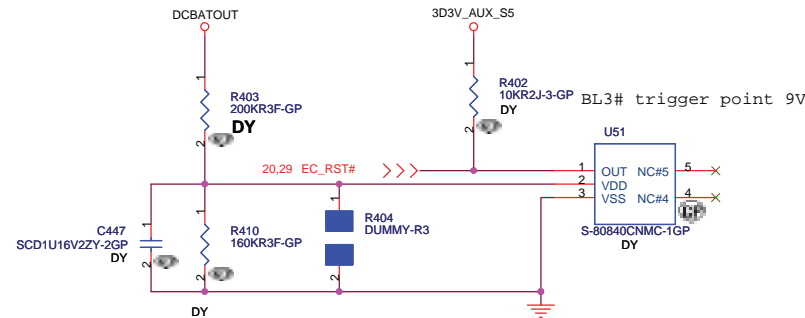


CAPACITY BUTTON

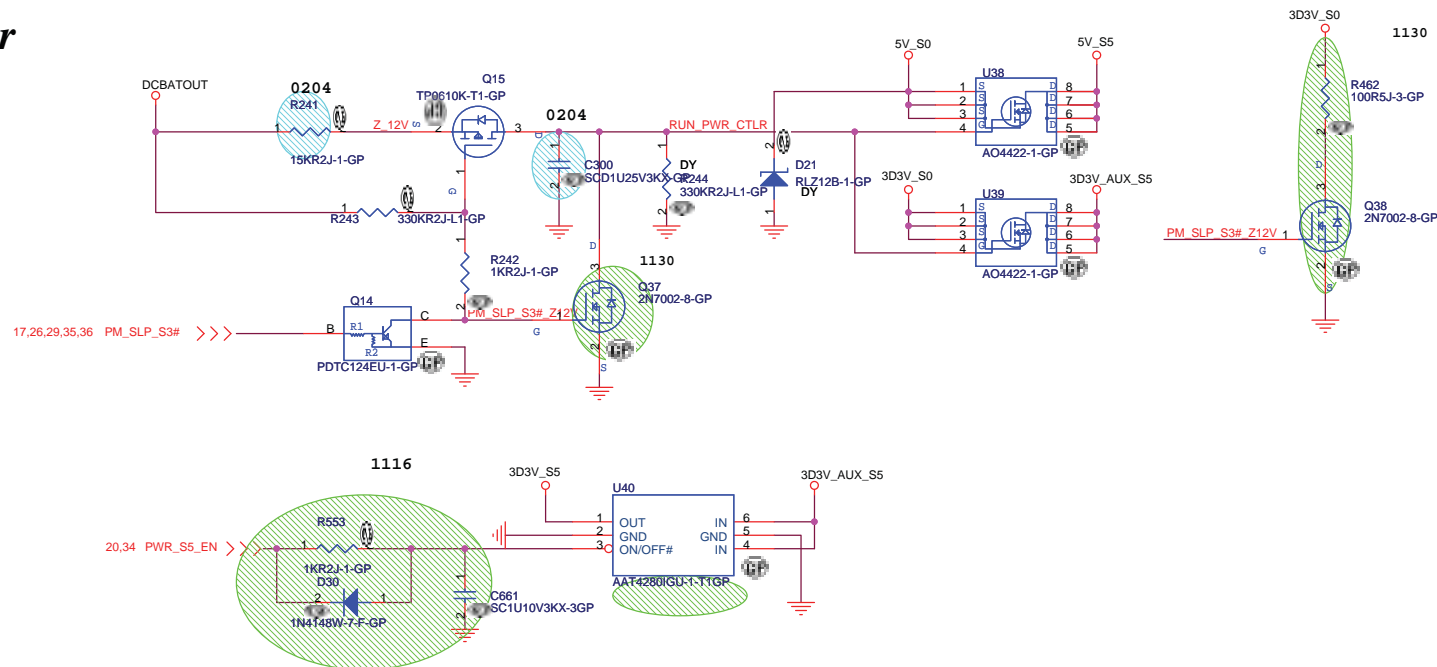


<Core Design>





Run Power



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

PWRPLANE&RESETLOGIC

Size
A3

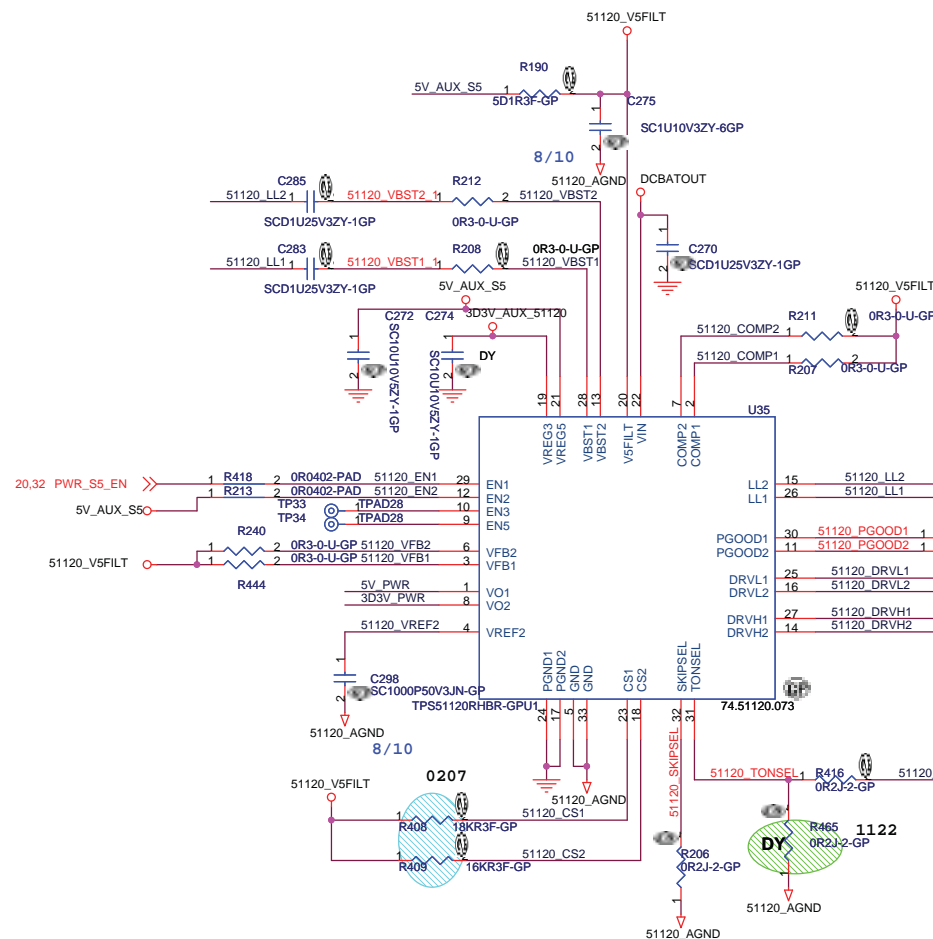
Document Number

Akita

Rev
SD

Date: Friday, March 31, 2006

Sheet 32 of 39



$I_{omax}=11A$
 $Q_g=9.8nC$,
 $R_{dson}=20\sim 25mohm$

$I_{omax}=11A$
 $Q_g=9.8nC$,
 $R_{dson}=19.6\sim 24mohm$

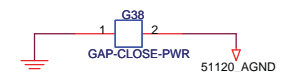
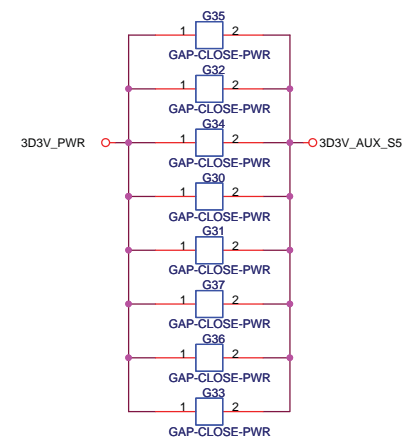
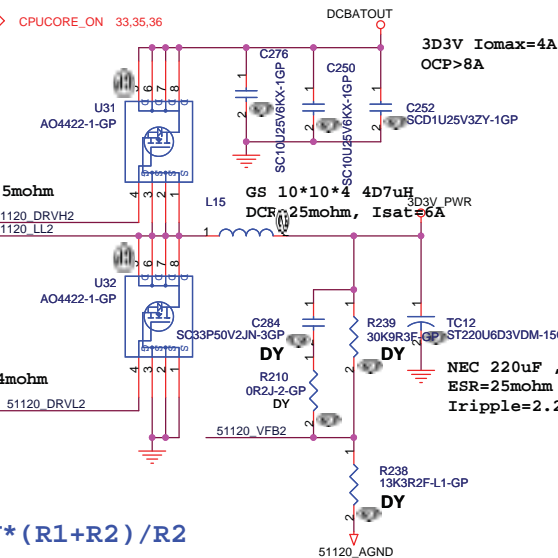
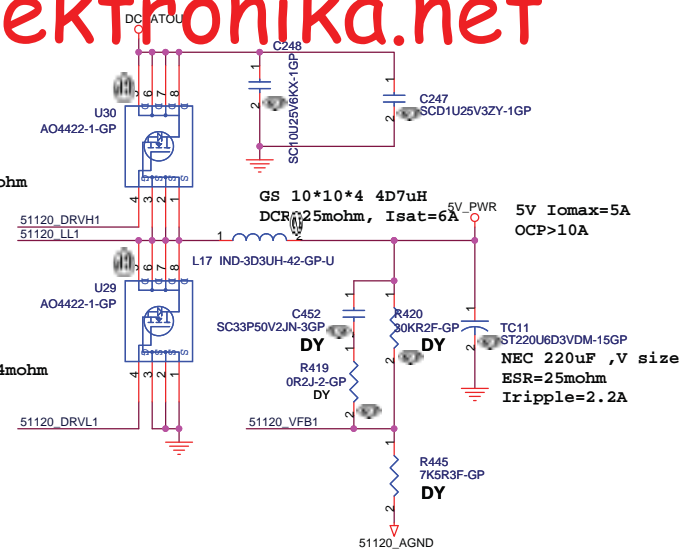
$I_{omax}=11A$
 $Q_g=9.8nC$,
 $R_{dson}=20\sim 25mohm$

$I_{omax}=11A$
 $Q_g=9.8nC$,
 $R_{dson}=19.6\sim 24mohm$

$$V_{out}=1V \cdot (R1+R2) / R2$$

For TPS51120,
 $V_{out}=5V$

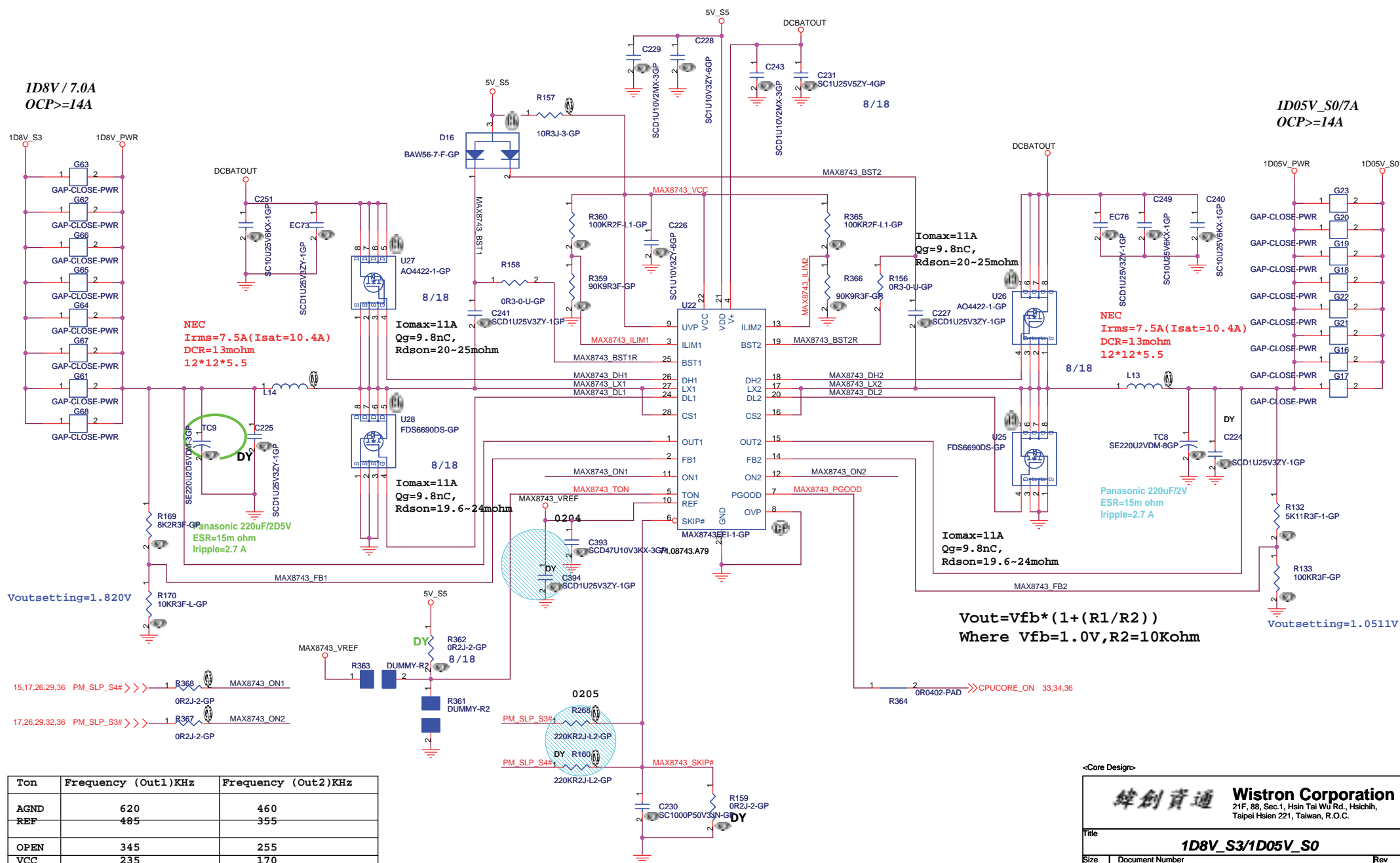
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
 2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
 3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
- $V_{out}=3.3V$
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
 2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
 3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.



<Core Design>

<http://hobi-elektronika.net>

1D8V / 7.0A
OCP>=14A



Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

1D8V_S3/1D05V_S0

Size
A

Document Number	
-----------------	--

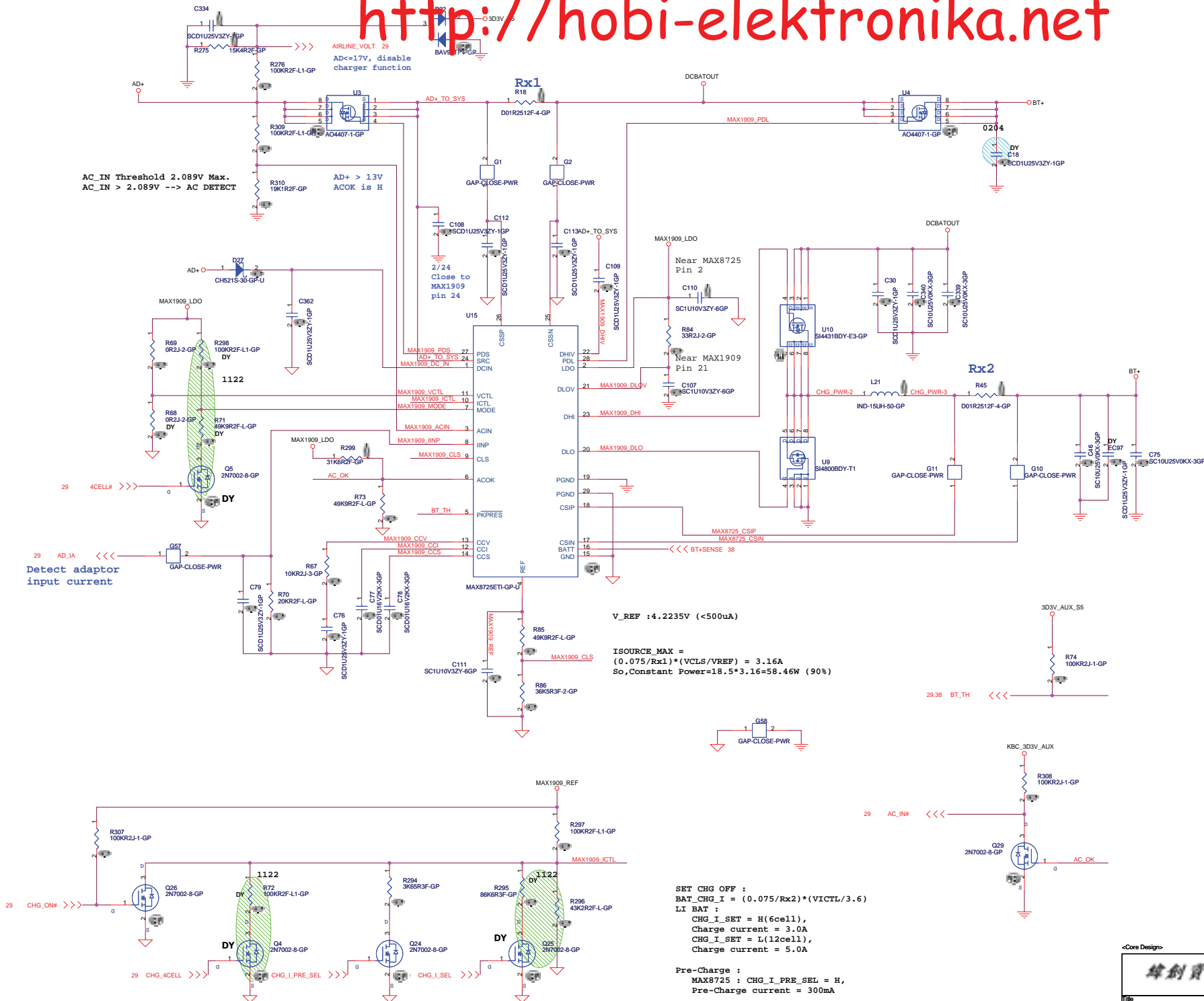
Akita

SI

Date: Friday, March 31, 2006

Sheet 35

39

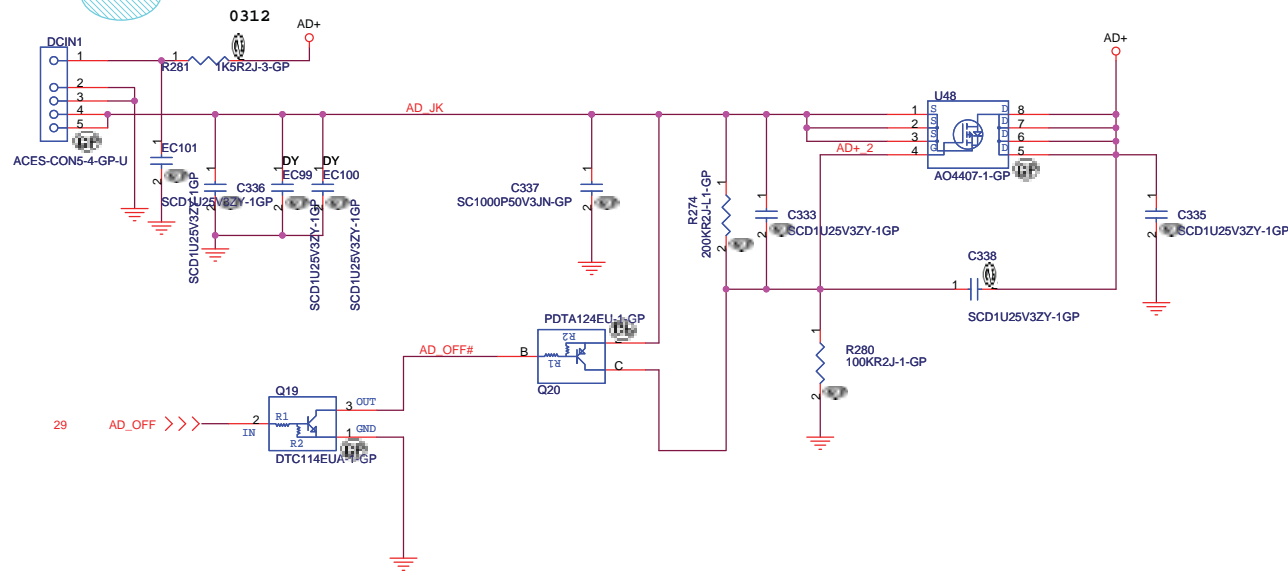


```

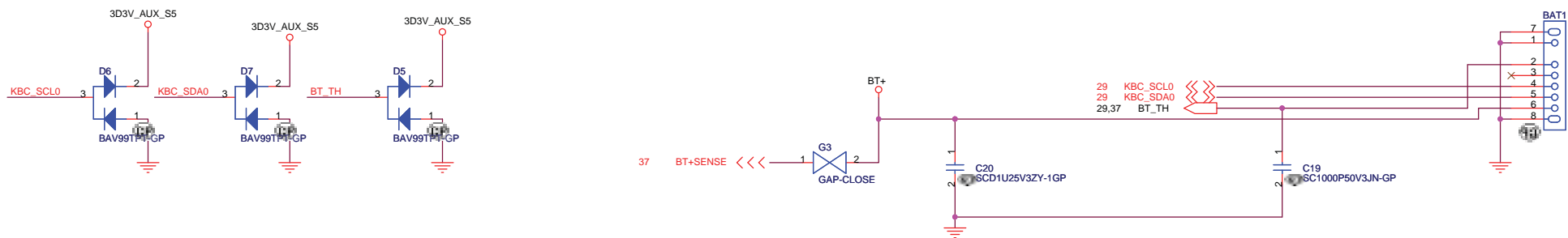
SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6
LI BAT :
    CHG_I_SET = H(6cell),
    Charge current = 3.0A
    CHG_I_SET = L(12cell),
    Charge current = 5.0A

Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA

```



BATTERY CONNECTOR



<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AD/BATT CONN			
Size A3	Document Number Akita		Rev SD
Date: Saturday, April 01, 2006		Sheet 38 of 39	

